# DEVELOPMENT OF A COMMUNICATION WITH PLC BY USING THE FL-NET AS AN OPEN STANDARD PLC LINK

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#### Abstract

We developed a control system for a linac interlock system of SPring-8 with MADOCA framework. The system consisted of a PLC, a PC with Linux, and the FLnet standard PLC communication interface. The FL-net is a standard interface and runs an open standard protocol, which is handled by the Japan Electrical Manufacturers' Association. The FL-net is a master-less token bus protocol on UDP/IP, and supports cyclic data transfer and message transfer. We mention about the linac interlock system, and an installation plan of the FL-net to the SPring-8 control system. We also report the results of the FL-net performance measurement together with its various features.

#### **INTRODUCTION**

In SPring-8, we use many types of Programmable Logic Controller (PLC) mainly for an interlock system. A serial communication line (RS232c) was used to communicate between the PLC and the SPring-8 accelerator control system. This was a unique solution to communicate between the accelerator control system and the PLC via same interface. One problem of RS232c was slow to transfer a data when we need to read a data within one second. A difficulty of maintenance was a problem too. In order to communicate between the control system and the PLC, we need to write a complex program to exchange binary data to ASCII character.

We evaluated an Ethernet interface of PLC. Each manufacturer of PLC has its own protocol, and some of them are not opened for end users. In addition several PLCs support to access an input/output register via Ethernet. It may generate serious problems for control system when a software bug hits wrong register. We need an open standard protocol if we use the Ethernet interface. Recently many manufacturers are promoting to bring Ethernet to factory floor devices such as robots, numerical control systems, PLCs etc. FL-net is one of the Ethernetbased open standard protocols for a factory floor network, and it makes consortium in Japan[1]. The FL-net based on Japan Automobile Manufacturers Association (JAMA) network requirements for factory floor devices, and was established as JEM standards in Nov 2000, and as JIS standards in Feb 2004. Main features of the FL-net are as follows:

- Physical layer is Ethernet.
- The newly developed 'FA link protocol' on UDP/IP meets a high speed, large quantity data

transmission.

- High speed cyclic transmission within 50msec at 32node
- Automatic participation or out-ring of a node (a station) is possible.
- Adopting a master-less token method and good RAS function.
- 8k words and 8k bits data are transferred by cyclic transmission.
- A message transmission service of 1,024bytes per frame is possible.

At the renewal of the SPring-8 linac interlock system, we planed to use the FL-net for communication between the PLC and the control system. The new interlock system was installed in summer 2004. We describe the system and its performance of a data transfer in this article.

## LINAC INTERLOCK SYSTEM

The linac interlock system handles several interlock sources to prevent serious damage of equipment. The twenty-five interlock modules are distributed around a klystron gallery. Figure 1 shows a bird eyes view of the klystron gallery, and the modules are installed on a gun. modulator sections and beam transport lines. All modules are connected as wired OR logic to form single interlock signal for linac beam operation. The old interlock system logic was made by TTL, and had no latch function of interlock source. This made us difficult to find a fault when a fault occurred in very short time. Also it was very difficult to change the logic to add components of accelerator. We replaced the interlock module by newly designed system. The new system is made from a Graphical Panel and PLC with the FL-net communication unit. We selected a FA-M3 from Yokogawa Electric Co.,Ltd.[2] for the PLC, and implemented a latch function and a logging system of interrupted sources on the PLC. The Graphical Panel displays a status of the interlock. The latched interlock can be cleared by manual using the Graphical Panel.

We used a Linux PC and PCI interface board to communicate with the interlock module via FL-net. For Linux operating system, we used RedHat Enterprise Linux 2.1[3] and implemented the MADOCA (Message And Database Oriented Control Architecture) framework[4] that is used to control the SPring-8 accelerator complex. We selected a FutureNet FL-PCI/V2 from Century Systems, Ltd[5] as PCI board of FL-net interface. On this board the FL-net protocol was implemented on a firmware. It means a real-time performance is determined by not software but hardware. It is not preferable to implement the FL-net protocol by software because a real-time characteristic of the Linux is not enough.

We use 10BASE-FL with 62.5  $\mu$ /GI optical fibers for connection between PLCs to avoid electro-magnetic interference. Figure 2 shows a schematic view of the network system. We use 10Mbps stackable HUBs. A

10BASE-T is used for the FL-net connection of the Linux PC.

An interlock status was stored into the database of the SPring-8 accelerator control system by using the MADOCA framework. The Linux PC has a function to reset an interlock via the FL-net. The function is controlled from the central control room of the SPring-8.



Figure 1: A bird eye view of the klystron gallery. The modules are installed in the control rack of a gun modulator, a buncher, S-band modulators and beam transport lines. The red line shows an optical fiber for FL-net.

## PERFORMANCE

We measured a performance of cyclic data transfer time with twenty-two PLC nodes and one PC node. The physical layer of the FL-net is the Ethernet, so that standard analyzers and standard test tools are available. We used the Ethereal with a FL-net extension[6] to analyze a performance, as shown in Figure 3. It could decode the FA link protocol header information. The solid square of Figure 4 shows a cyclic data transfer time with 100 words data per node, and the error bar shows



Figure 2: A schematic view of the network system for FL-net.

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49 0.036363 192.168.250.1 192.168.250.255 FACN Cu	clicHeader(1->2)
	kenHeader(1->2)
51 0.037904 192.168.250.2 192.168.250.255 FACN Un	defined Frame(2->250)
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Figure 3: A screen shot of the Ethereal with FL-net extension.

 $1\sigma$  deviation. The cyclic transmission is 33msec at twenty-three nodes. The result agrees well with the design specification of the transfer time 50msec at thirty-two nodes of the FL-net. The solid triangle shows a cyclic data transfer time with a message transmission service of 1000btyes per frame. The message was transmitted as loop-back test and peer-to-peer communication. This shows an effect of the message transmission service to a cyclic data transfer time.

### PLAN

Based on the successful operation of the FL-net we decided to use the FL-net as the standard to communicate between a PLC and the control system. We have several plans to replace a serial communication to the FL-net. An interlock system for top-up operation is one of the systems to be modified. When we run the SPring-8 with top-up operation mode [7] we have to count electron beam charges injected to the storage ring, and estimate beam loss of injection. All the data monitored by beam current monitors are taken by a PLC with serial line, and logged into the database every second. Total size of the data is about 700bytes, and it takes about 300msec to transfer the data from the PLC to the control system. Because a ramping time of the booster is about 600msec, the net time interval of the data logging is very tight for 1Hz beam injection. This interlock system uses the Mitsubishi Electric Co.,Ltd.[8] Q series PLC. We will evaluate the O series in spring 2005, and the PLC communication interfaces will be replaced by FL-net



Figure 4: A plot of the cyclic data transfer time. A solid square shows cyclic time with 100 words data per node and a solid triangle shows cyclic time with a message transmission service of 1000btyes per frame.

modules in summer 2005.

Other system is a linac modulator control. It uses Toshiba Corporation T2 series[9]. We have already started an evaluation of T2 series FL-net module, and no serious problem to communicate with the control system has been observed.

#### **SUMMARY**

We replaced the linac interlock system from the old system, made by TTL logic, to the new PLC system with the FL-net. The FL-net is based on Ethernet physical layer, and plays open standard factory network. The FLnet was used for communication between the PLC and the SPring-8 accelerator control system. We developed the FL-net communication software with Linux PC and PCI board, in order to fit the MADOCA framework.

We measured the performance of cyclic data transfer time of the FL-net with or without a message transmission service. The results show that the highspeed transmission of large quantity data is possible. We use the FL-net as the standard interface to communicate between PLC and the control system.

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