DISTRIBUTED DAC SYSTEM-AREA NETWORK WITH EMBEDDED SBC AND DSP-BASED NODES

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INTRODUCTION SAN ARCHITECTURE

From 80-90's PC boards were limited by large scale integration (LSI) chips, which latter was transferred to a single-chip microcomputer (DSP), Single Board Computers (SBC) and Embedded Nodes. PC/104 (Plus) modules was example of Embedded processor made from PC desktop and laptop components, supported by embedded Linux, and using the PCI bus for board-to-board connections (120-pins). Some Microprocessor components have very much pins in standalone 16/32-bit PCI -based systems based within single board or passive Buses (VME/VXI, cPCI/PXI). The VME bus allowed 16-bit data transfers on the 3U-form factor, and full data bus bandwidth - between 6U modules. The cPCI/PXI **(3U)** format is more effective, its performance is superior to VME/VXI and enables system flexibility extending the PCI slot limit from 4 (to 8) modules. Single Board Euro 3U-standard is compact platform, but SBC with Input-Output Modules (half-size) on passive 3-4 slots PCI can be effective for compact Embedded DAQ and Control Systems applications. Embedded SBC with Serial interfaces (USB, Fire Wire, CAN, Ethernet) used for modern compact node interconnections with less pins. Possibility of Microelectronics is became more power and the requirements to performance of DAC-systems in Experimental Area are becoming more and more higher each year.

Accelerator Control and Experimental DAC Systems for Fundamental and Applied Researches are joint in Experimental Area according to proposed Multi-level System-Area-Network (SAN) Model for Data Acquisition and Control, which includs next data-flow processing:

1) Data-Flow processing as reduction of events in volume and frequency oneach level:

$$\mathbf{DF(i) = I(i) * F(i)},$$

where: **I(i)** – Event Data Volume on i-level
F(i) – Frequency of Data Events on i-level

2) Data-Flow Volume Reduction on i-level

$$\mathbf{I(i) = Q(i) * I(i-1),}$$

where: **Q(i)** – Event Volume Reduction Coefficient on i-level of Data processing.

3) Data- Flow Event Frequency Reduction on i-level

$$\mathbf{F(i) = R(i) * F(i-1),}$$

where: **R(i)** - Event Frequency Reduction Coefficient on i-level of Data Processing.

4) Control Data Volume on i-level

$$\mathbf{C(i) = K(i) * C(i-1),}$$

where **C(i)** – is Control Data Volume on i-level of the information Model.
K(i) – is Control Data Reduction Coefficient on i-level of the Model

Data Acquisition and Control (DAC) Systems with Modular Architecture should be integrated in flexible System-Area Networks (SAN) with Embedded SBC and DSP-based nodes, based on PC-compatible Core and High-performance network protocols on the base of proposed model.

Two approaches to Distributed compact Modular System Architecture are discussed below.

COMPACT SBC-BASED MODULAR SYSTEM-AREA-NETWORK (S AN) ARCHITECTURE

The first approach to SAN Architecture is construction of effective (price/performance) System Architecture on the base of week interactions between Distributed SBC and DSP-based modules. The advanced platform to realize Effective Systems Architecture is compact Node with 2-3 PCI-slots Bus for SBC and DSP-based modules (DAC) and signal conditioning front-end Electronics, integrated in Distributed Terminal nodes as a Real-time Systems.

This basic approach consist of compact Embedded SBC and DSP-based modules and tradition network with week interactions between Cores is more effective, as much more expensive of cPCI/PXI-based platform. Modern modular Monitoring and Control Architecture based on IP-protocol (tradition Ethernet 10/100/1000) is good decision for Distributed system. System Architecture with distributed Control Terminal Nodes (Compact Terminal Station) for Signal Processing and Control in Real-time on the base of Ethernet is proposed and discussed.

Control Terminal System TCS-node can work as autonomous Device or as Distributed Nodes in integrated System Architecture. It can provides Signal Registration (Monitoring/Diagnostics), Signal Processing and Visualization. Graphical User Interface was developed for registration events, monitoring and control. A lot of compact Terminal Stations can be connected by LAN with servers and supervisor.

Supervisor Control Station (node), which provides control, test and monitoring of each remote Terminal Nodes, can be used in more complex signals analysis from a number of distributed Terminal Stations. Signal Modeling and Simulating are additional Contriol Terminal functions for testing, modelling and simulating of real objects signals (internal embedded signal

generator) or by special generator station (as external precision Signal Generator) Nodes. Virtual Generator Model software should supports complex modelling and simulating with help of internal or external generator nodes on System inputs for Real or Modelling Event Data file, Internal or External Event Signal Simulating in Real-time on the given node. Example of pilot system was developed for power net event registration.

DISTRIBUTED MEMORY MULTIPROCESSOR SYSTEM ARCHITECTURE

The second approach is advanced high-performance 64-bit Distributed Memory Architecture Model for single or multicore Processors with Flexible System Topology, following requirements of Real-time Data Sources for effective Experimental Data Processing (2D or 3D or Tour), based on strong interactions between Distributed nodes. Distributed-memory Architecture provide direct access to distributed memory, and its topologies can be effective for Data Processing in Real-time. Advanced Joint Architecture can be especially effective for high-performance Systems on the base of new generation 64-bit Intel multicore processors, integrated in Advanced Distributed modular Nodes. Both approaches can be constructed as Effective High-performance Flexible Modular System-Area-Network for DAC applications.

Distributed-memory Model for Multiprocessor system with SAN-architecture is fundamental to support high-performance parallel-pipeline data processing (computing) in RT-applications. Direct access any processor to any memory in single address space of the Integrated System is working like SMP model.

Cache coherency in multi-processor systems is required to support data availability for all processor during distributed data processing (parallel computing) in real time, as a problem of distributed multiprocessor systems, which include many processors, attempting to modify a single datum or holding their own copies of it in their cache at the same time. Hard disks should be used as reliable distributed external memory near each processor module. Tradition Ethernet can be used as basic interconnections in different Control applications and as additional communication media for system initializing and administration. Interconnections in such system are based on parallel-pipeline packet transactions between distributed Nodes.

Technology Independent advanced System Architecture should be ready to support a new technology, including multicore processors and provides long living time of systems and up-grading modules on different level. As Example, SCI-based network Architecture with high-modular structure not depend on changing Technology and should consist of compatible standard module of different vendors. The complex Architecture with weak and strong interactions between Distributed single or multicore Nodes can be used effectively, where weak interactions (tradition Ethernet) can be used for installation, remote access, maintenance and control, but strong interactions – only for high-performance Data Acquisition and Processing in Realtime. The Joint Approach to Complex System-Area-Network (as SAN-DAC Applications) on the base of Jouint model Architecture for Advanced Distributed Modular Real-time Systems (for Advanced Experimental Area) are proposed and discussed.

RESUME

1. According to Multilevel Model of DAC-System The Distributed System-Area-Network Architecture is Proposed with weaknand stronhinteractionbetweenprocessor Core.

2. Compact Teminal DAC Stations can be constructed on the base of 3-4 slot PCI bus and can be use as single station or Integrated part of Distributed system with tradition network Ethernet 10/100/1000 for Monitoring and Control Applications.

3. High-performance Data Acquisition can be efective constructed on the base of SAN-Architecture with Distributed memory and SCI.

4.Complex SAN-Architecture approach can be used for new high-performance system with muliticore nodes using both weak and strong interaction, where strong interacting nodes can be used for DAQ and Data-flow Processing and Weak interactions will be used for remote access and maintanence installation.

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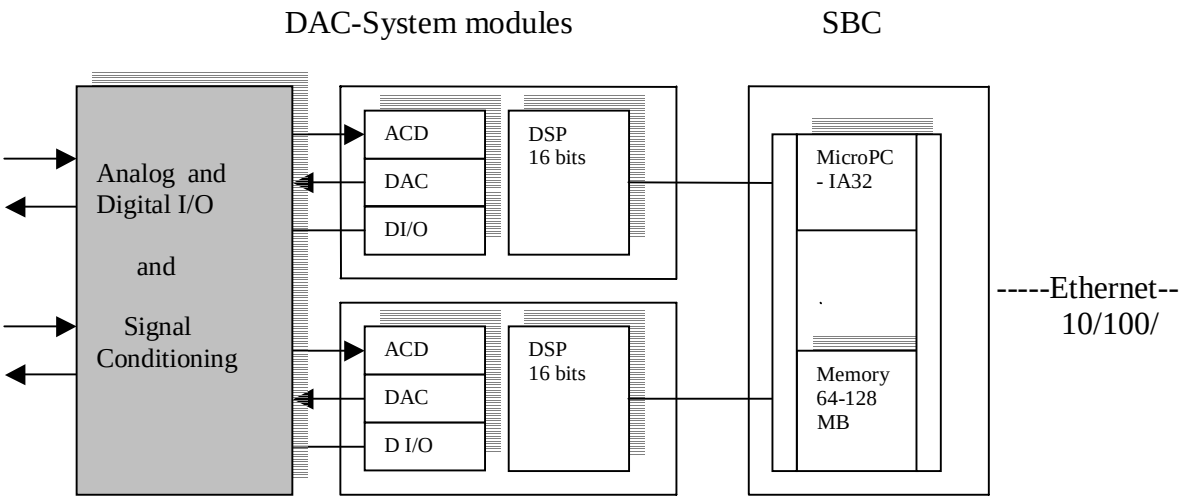

Figure 1: Compact Terminal Station with DSP-based DAC Modules (for Measurement and Control) with Signal Conditioning device (SCD), connected to SBC by Parallel or Serial (USB) interfaces.

Figure 2: Example of Supervisor and Servers Slim PC node.

Form Factor for AMD® Athlon™/Duron™ Processor
Ethernet 10/100, USB ports x 4 (2+2), Micro ATX Form Factor, Integrated Audio / Video

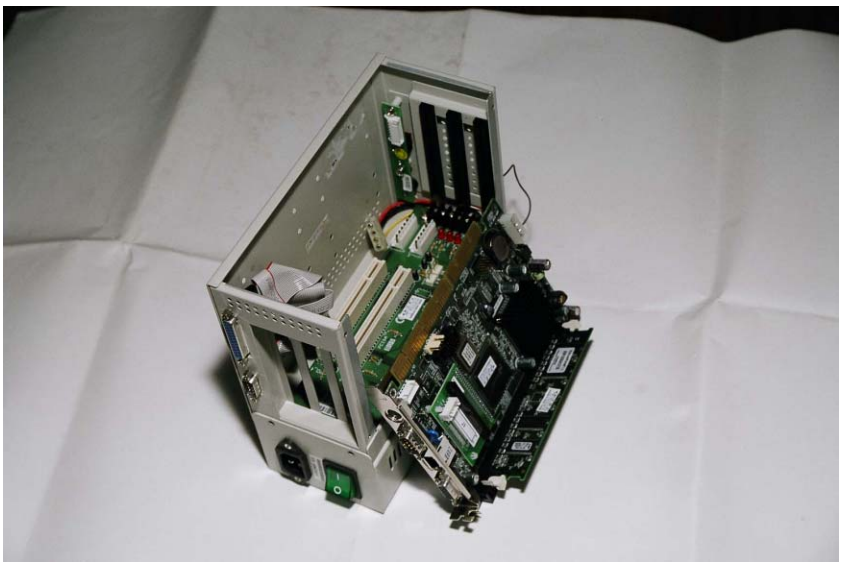

Figure 3: Example of compact Node with SBC and DAC Modules on 3-slots PCI bus.

Figure 4: Example of Signal Condition Device (SCD) with embedded modules SBC and DAC.

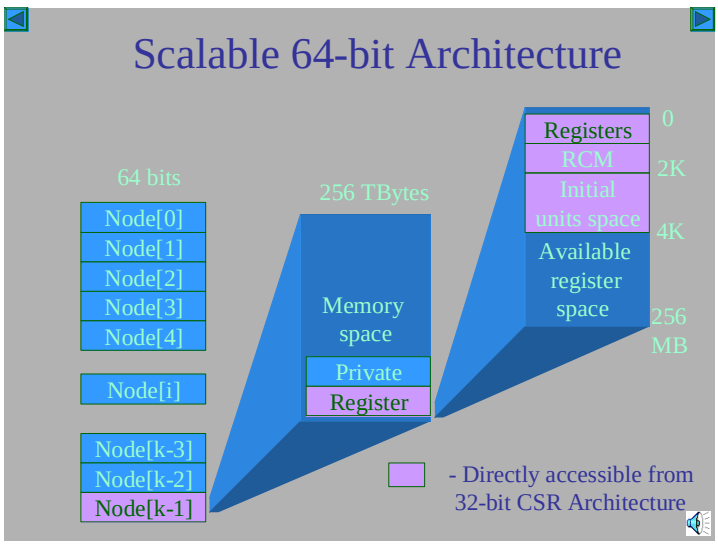

Figure 5: Advanced Distributed Menory Architecture.

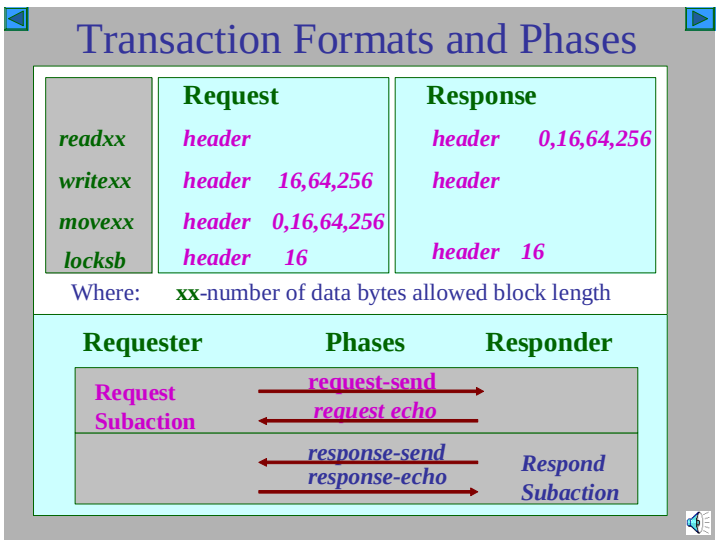

Figure 6: Packet Transaction Formats in SAN with Distributed Memory.