

# Solid-State Modulator R&D at LLNL

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RPIA

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**NLC - The Next Linear Collider Project**

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10/15/02  
Ed Cook  
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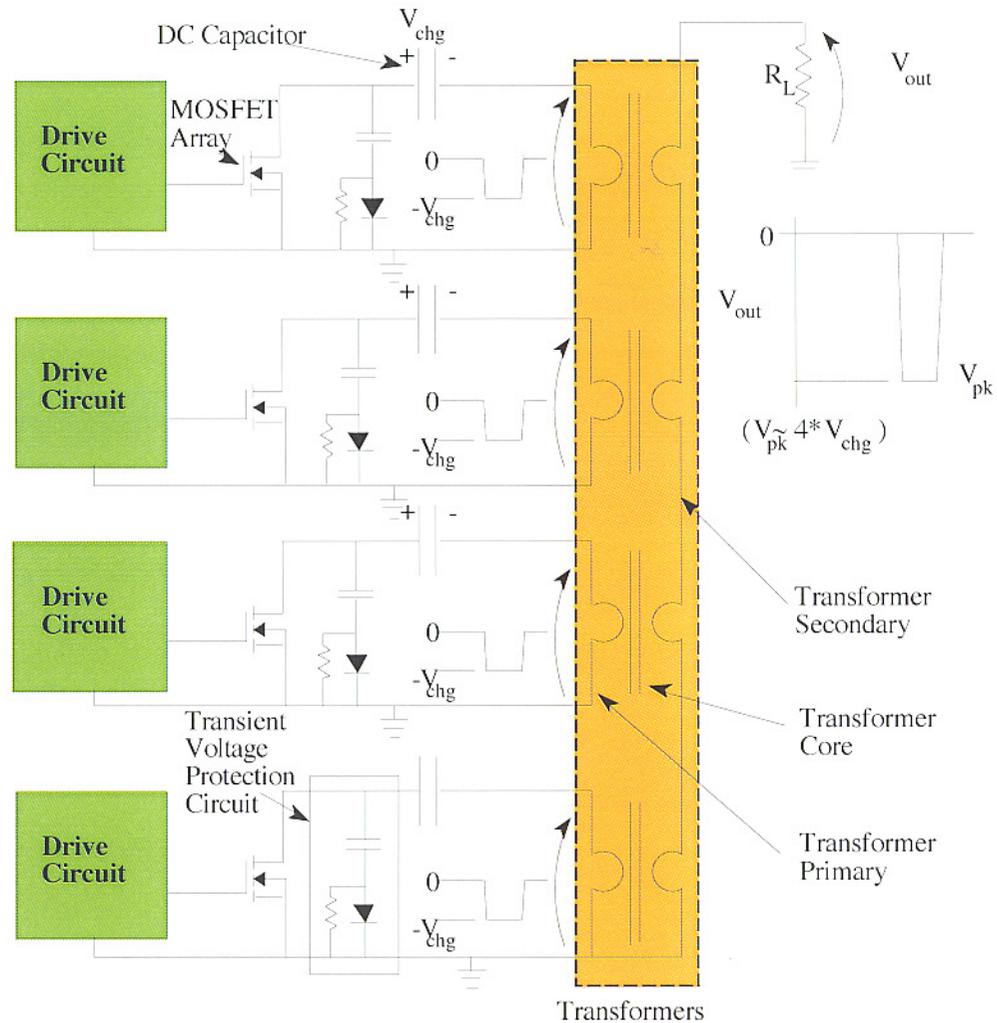
# Solid-State Pulsers

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- Inductive Adder Pulsers
  - Circuit Topology
  - Advantages/Issues
- Fast Kicker Pulser for Linear Induction Accelerator
  - Pulser requirements
  - Test Data
- Fast Kicker Pulser for Proton Ring Accelerator
  - Pulser Requirements
  - Test Data
- Klystron Modulator NLC (Next Linear Collider)
  - Requirements
  - Test Data
- Summary



# Simplified Schematic of Inductive Adder



# Adder Circuit Topology

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- Advantages
  - All drive components ground referenced
  - No high voltage grading required
  - Pulse format defined by programmable pulse generator
    - Pulse width agility
    - Burst frequency agility
    - High burst frequency >1 MHz
  - Modular - adder consists of stack of identical modules
    - All modules switch same voltage/current
    - All modules triggered simultaneously
    - Scalable to higher voltages by adding modules



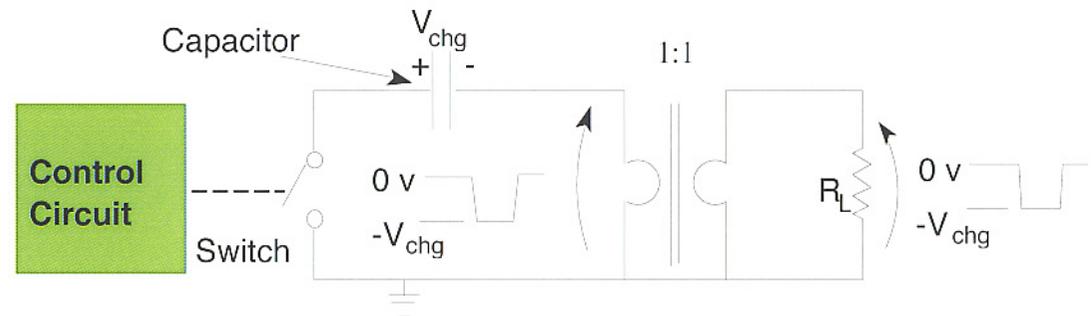
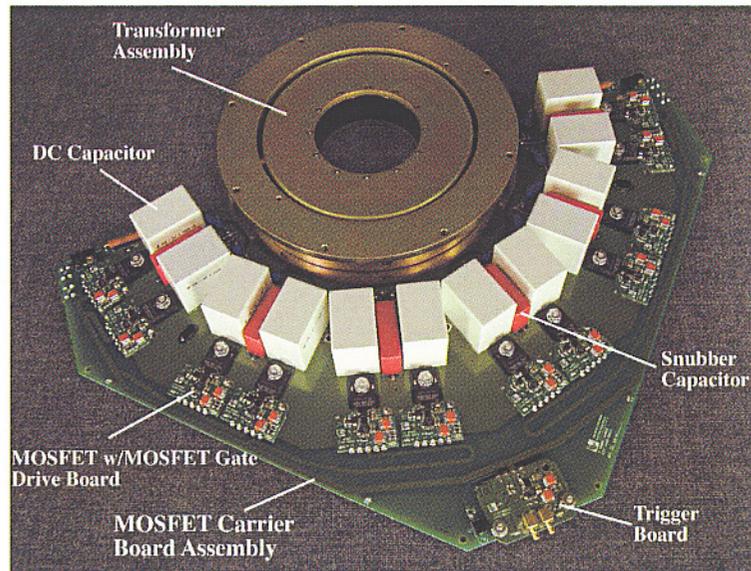
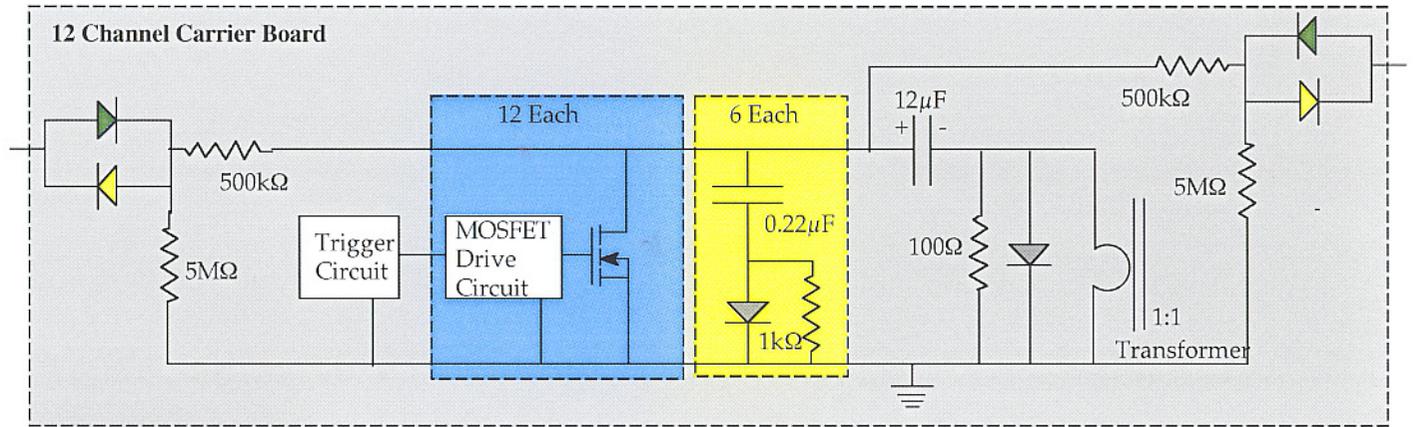
## Adder Circuit Topology

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- Issues:
  - Each module handles full load current
    - May require many parallel components (solid-state devices, capacitors, etc.)
    - Parallel switching devices must have low jitter on both turn-on and turn-off
  - Requires very small loop inductance (capacitor, switch, and transformer)
  - Requires very fast opening switch that can interrupt full load current and survive fault currents
  - Fault currents can be very large (adder modules are very low impedance)
  - Cost

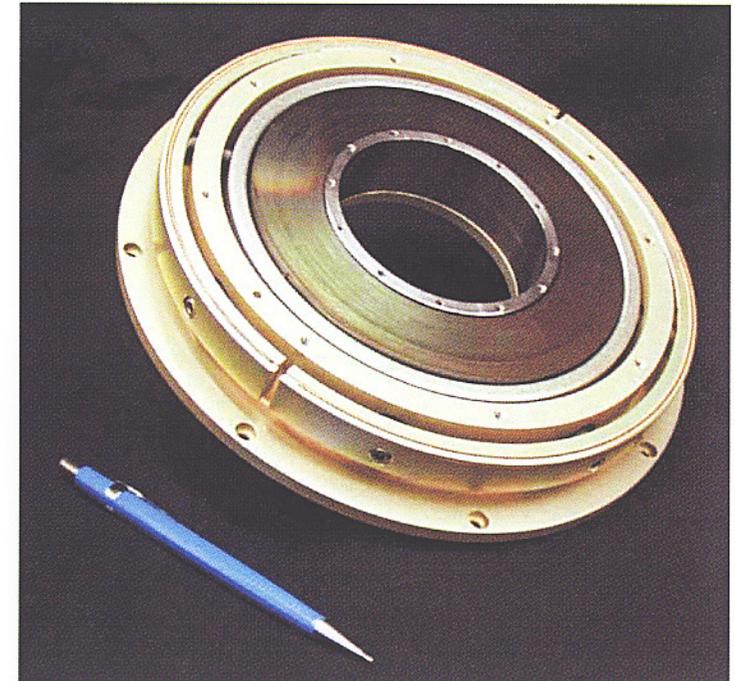
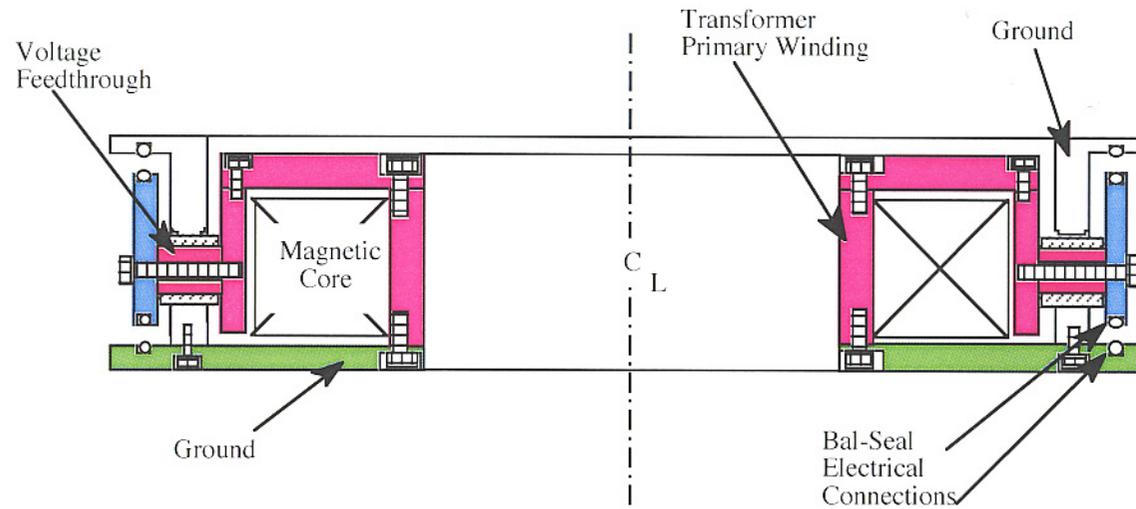


# Circuit Schematic - Adder Drive Bd.

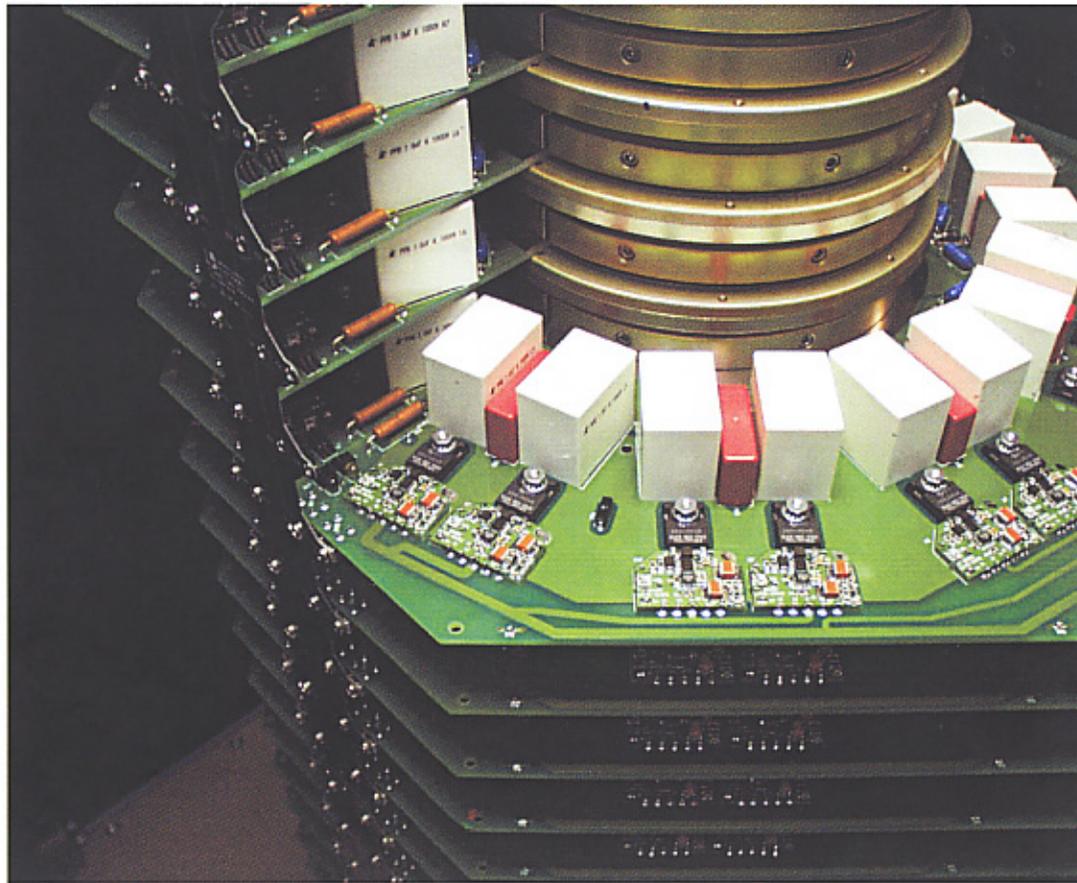


**Simplified Adder Drive Ckt.**

# Adder Cell Design



# Prototype Adder Assembly



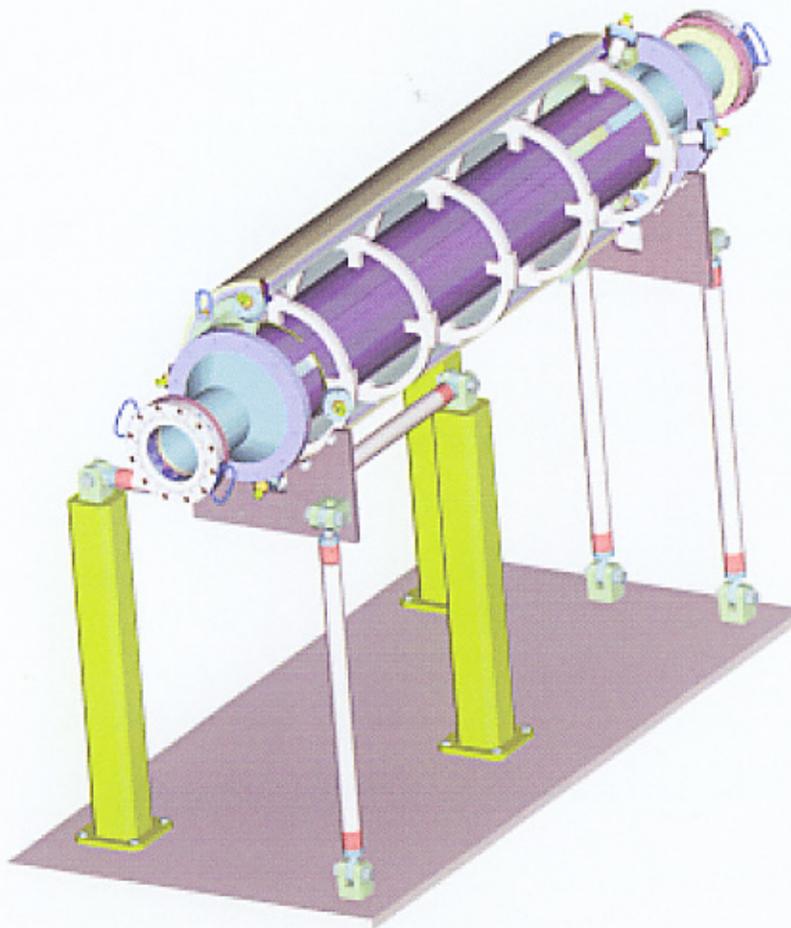
## Fast Kicker to Chop Pulses out of 20 MeV, 2kA, 2 $\mu$ s Electron Beam from Linear Induction Accelerator

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- Fast kickers installed in accelerator beam line feature parallel-plate, stripline geometry
- Fast kickers use the magnetic field and electric field created by fast high-voltage pulses of opposite polarity to steer the beam
- Kicker chops short pulses out of a 2kA electron beam of 2 $\mu$ s duration



# Fast Dipole Kicker - LLNL Stripline Kicker



## Kicker Pulser Requirements

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- $\pm 18\text{kV} \pm 10\%$  into 50 ohms
- 10ns rise and fall times
- 16 – 200ns wide pulses during burst: externally adjustable
- Multi-pulse burst
- Total pulse width of 500ns per burst
- Minimum intra-pulse spacing of 400ns



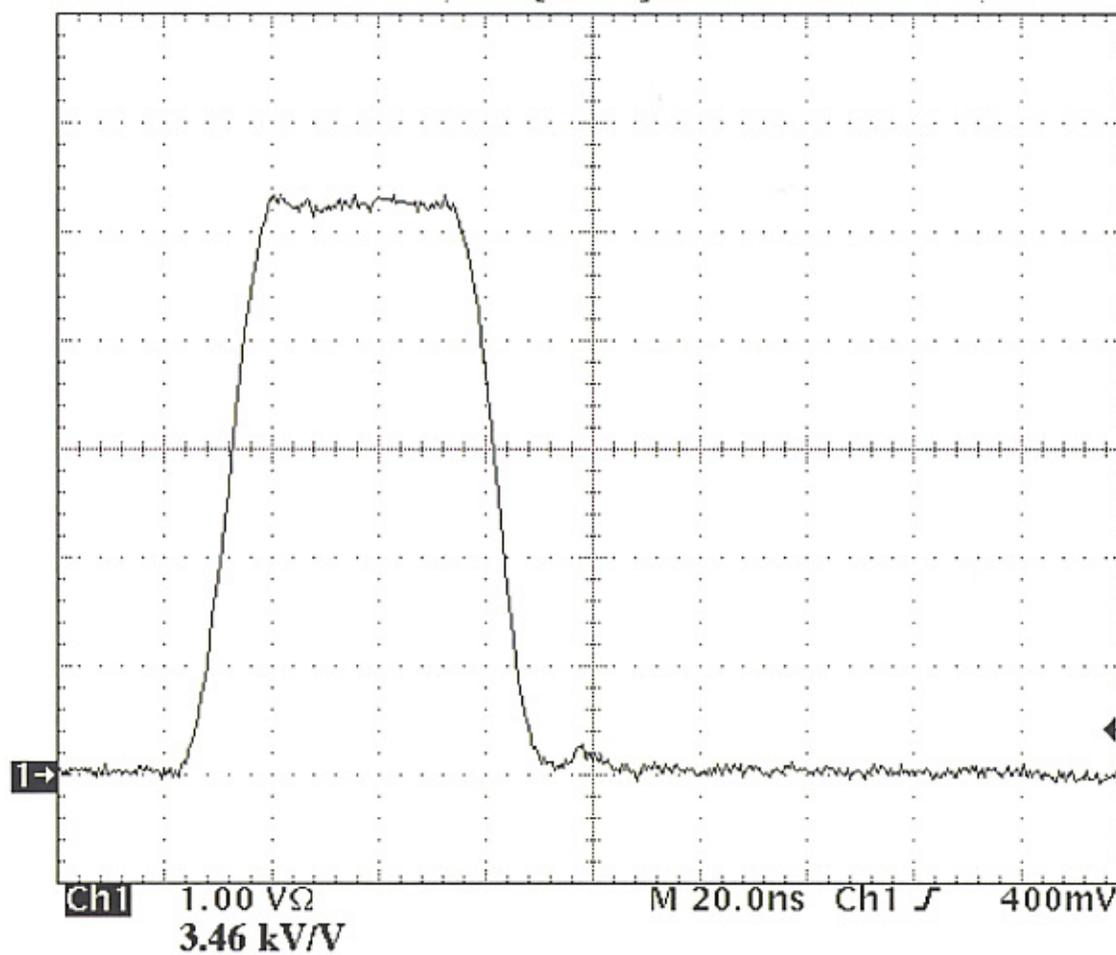
# $\pm 18\text{kV}$ Pulsers for Fast Dipole Kicker



# Output Pulse - 30 ns, 18 kV into 50Ω

Tek Run: 2.50GS/s

Sample **11192**



C1 Rise  
10.746ns  
Unstable  
histogram

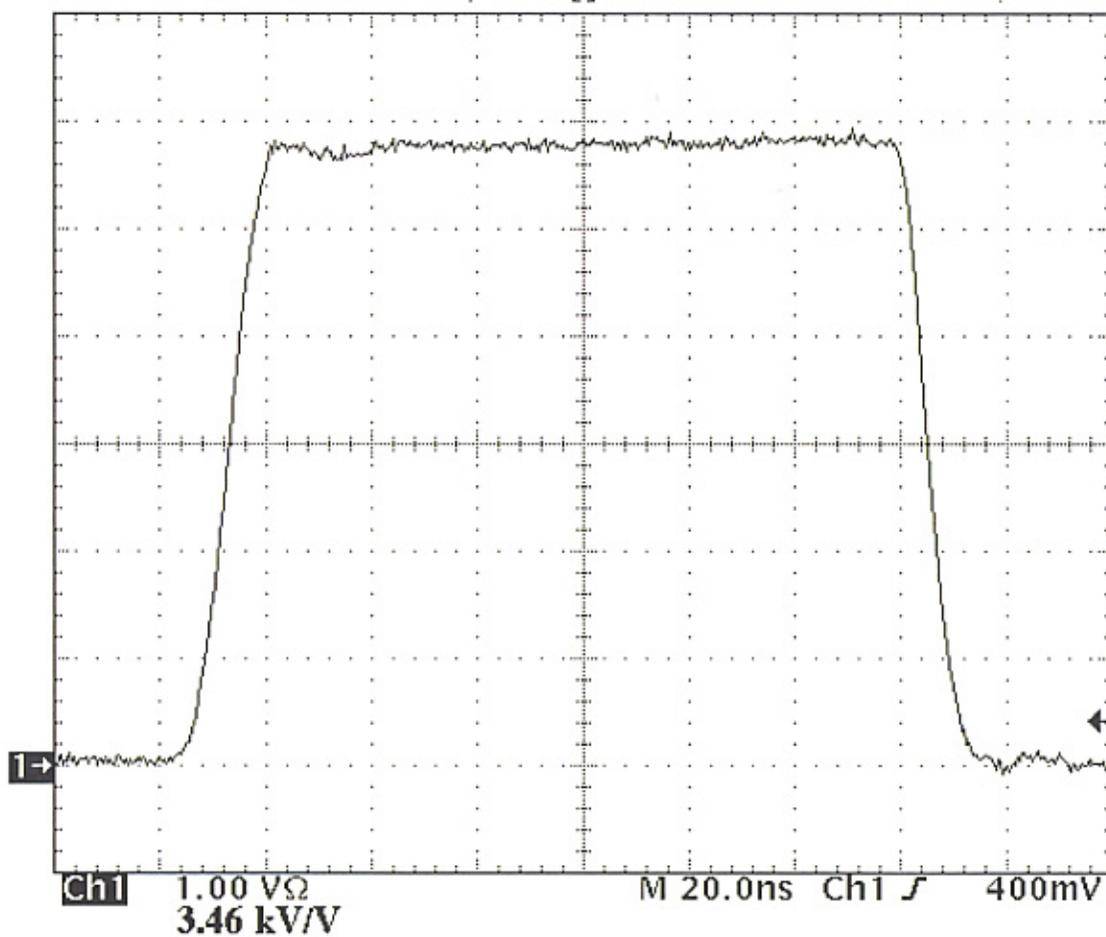
C1 Fall  
10.239ns  
Unstable  
histogram

5 Jun 2001  
09:40:46



# Output Pulse - 120 ns, 20kV into 50Ω

Tek Run: 2.50GS/s Sample **11102**



C1 Rise  
11.244ns  
Unstable  
histogram

C1 Fall  
9.074ns  
Unstable  
histogram

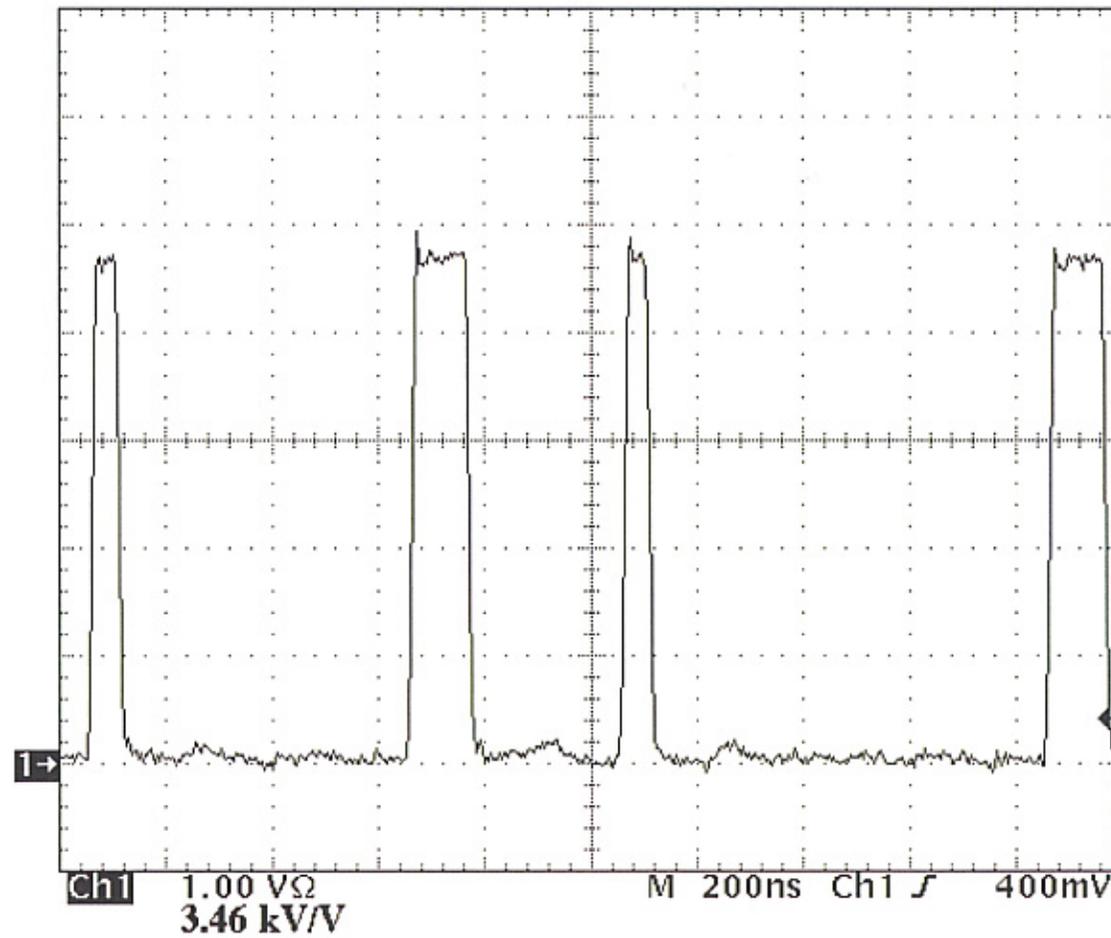
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14:11:57



# 4 Pulse Burst - Variable Pulse Width, Variable Burst Frequency

Tek Run: 250MS/s

Sample **1702**



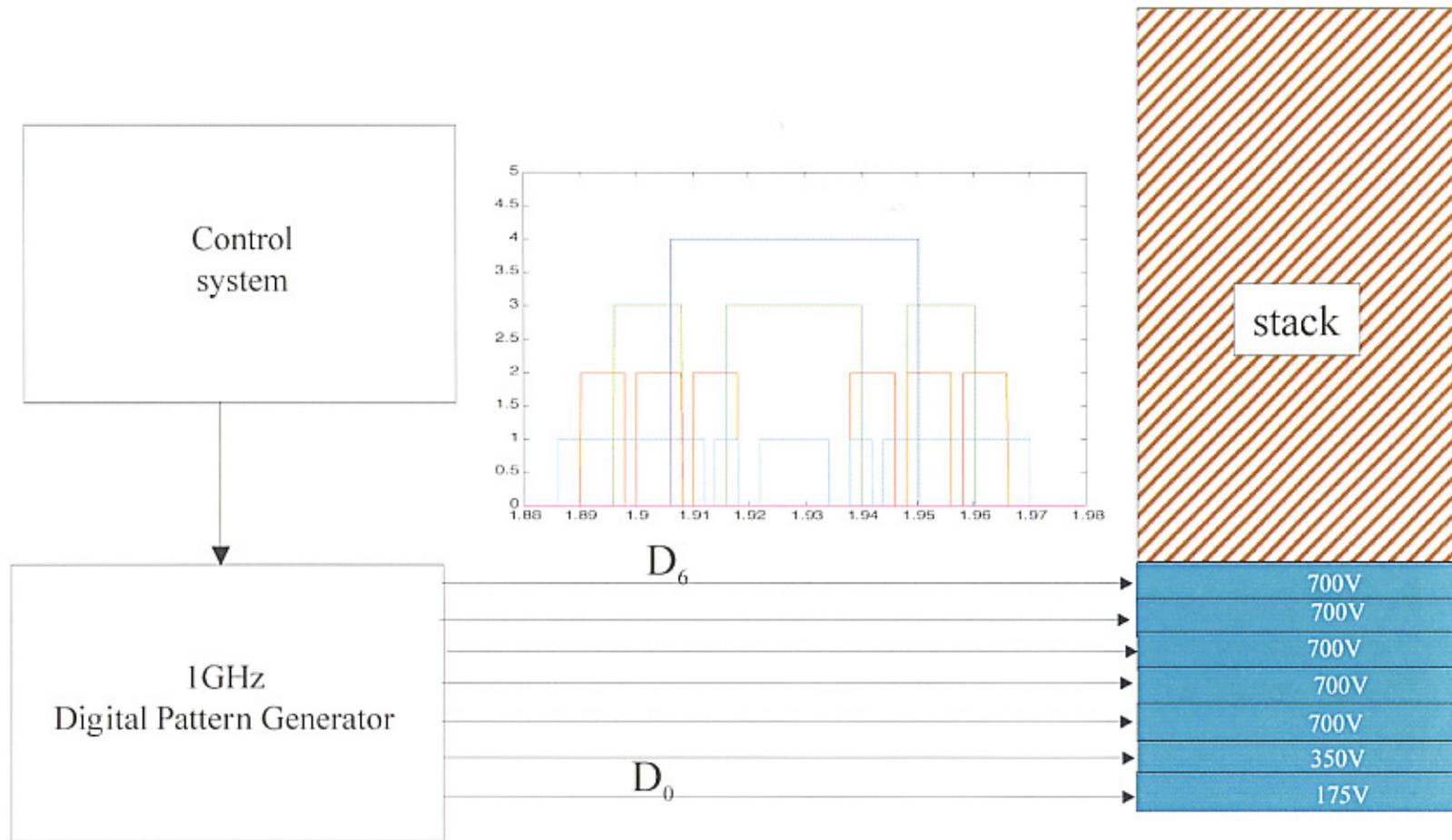
C1 Rise  
10.67ns  
Unstable  
histogram

C1 Fall  
12.40ns  
Unstable  
histogram

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13:39:00

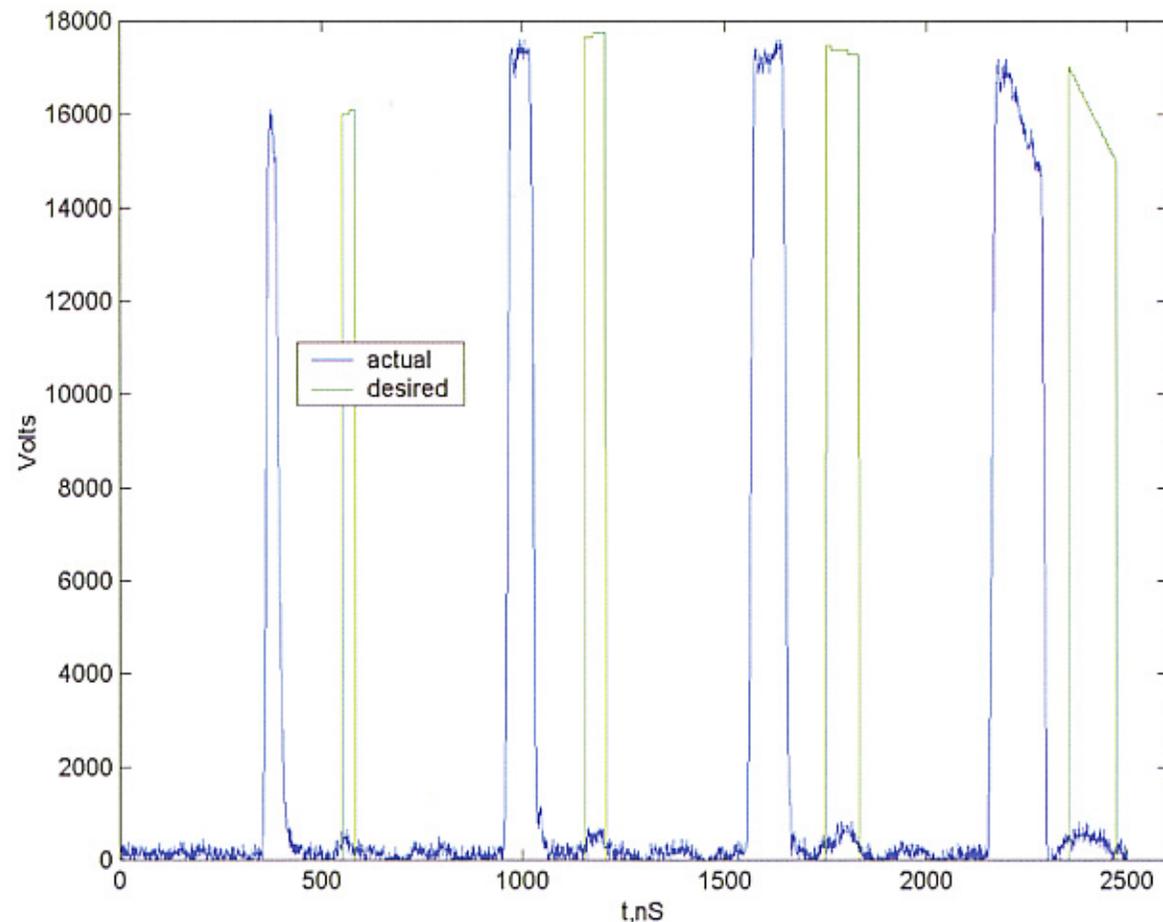


# Digital Modulation



# Modulated Multi-Pulse Burst

Four-Pulse Burst  
with Amplitude  
Modulation



## Fast Extraction Kicker for Proton Ring Accelerator

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- 50 GeV proton accelerator
- 24 proton bunches supported in ring
- Proton bunches have center-to-center spacing of  $\sim 200\text{ns}$
- Ring revolution time  $\sim 5\mu\text{s}$
- Full exploitation of accelerator capabilities requires an asynchronous extraction kicker system

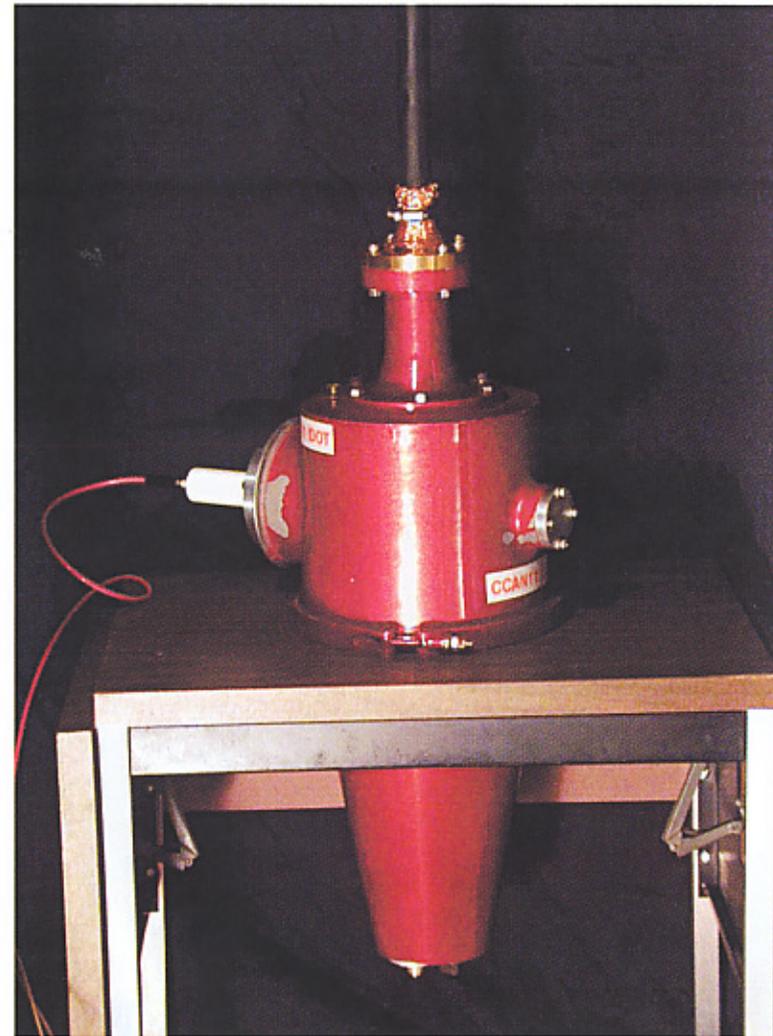
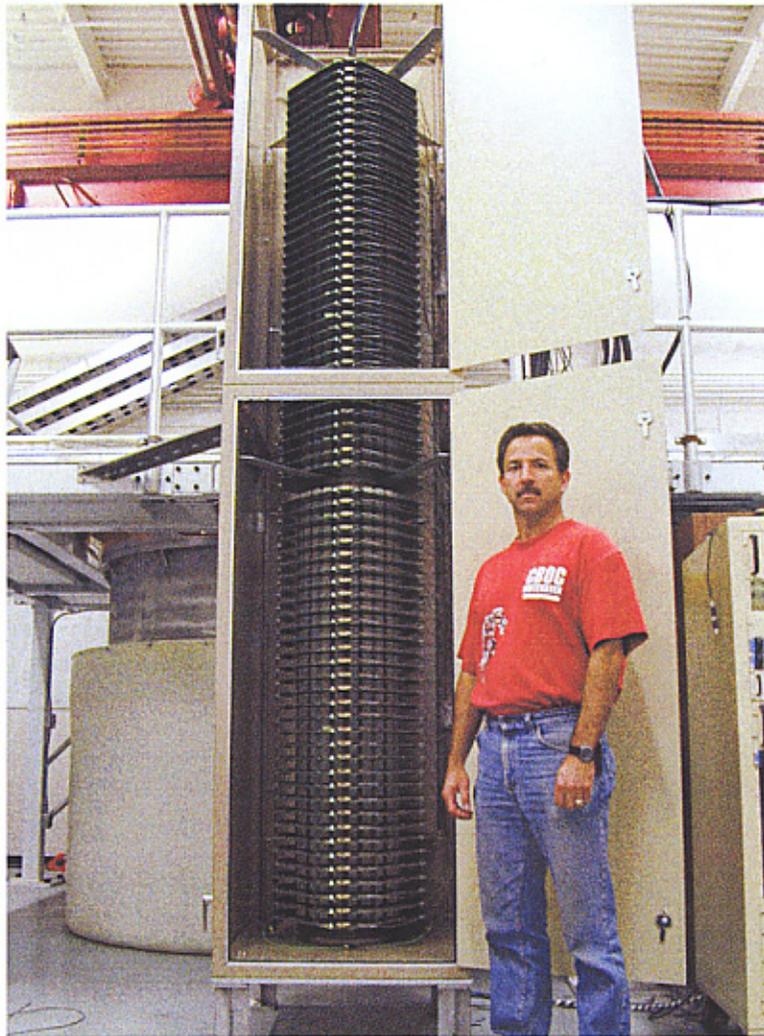


## Extraction Kicker Modulator Requirements

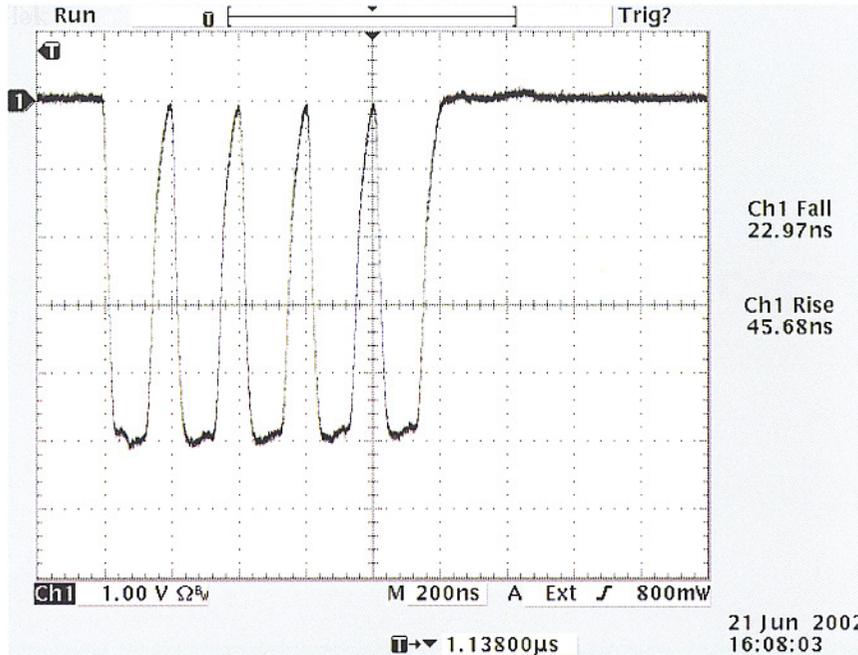
- 50 kV into 50  $\Omega$ \* (two pulsers required to achieve  $\pm 50$  kV)
- 24 pulse asynchronous burst w/max. 5 MHz burst frequency
- Minimum pulse flattop - 73 ns\*
- Maximum allowable risetime/faltime - < 64 ns (0-100%)\*
- Pulse flatness <  $\pm 1.0\%$  for each pulse\* and entire burst
- Intra-pulse voltage ripple - < 300V within 300ns of pulse falling edge\*
- \*To be demonstrated in prototype pulser



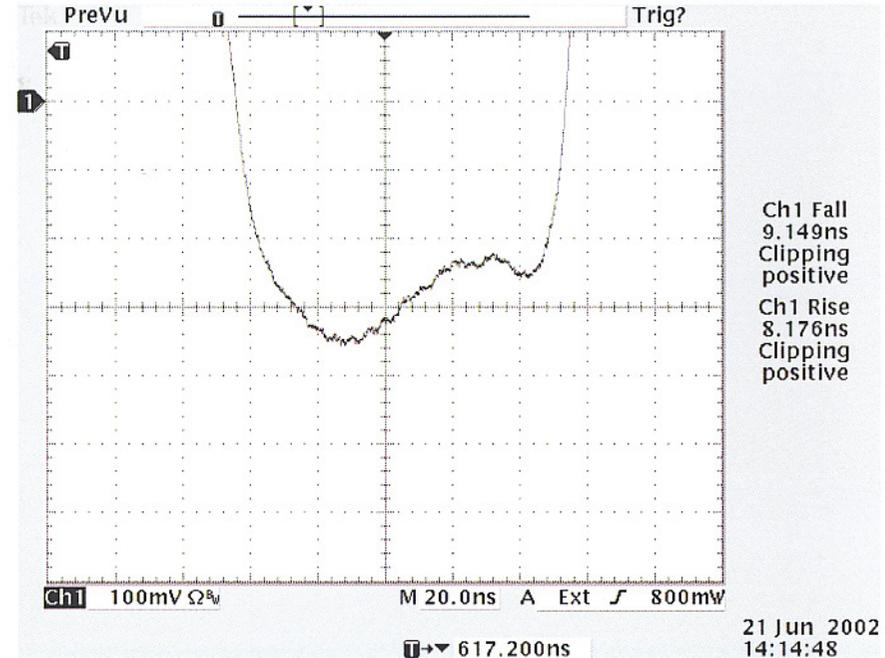
# Prototype 50kV Adder Stack Assembly and Dummy Load



# 50 kV, 5MHz Burst without Reset



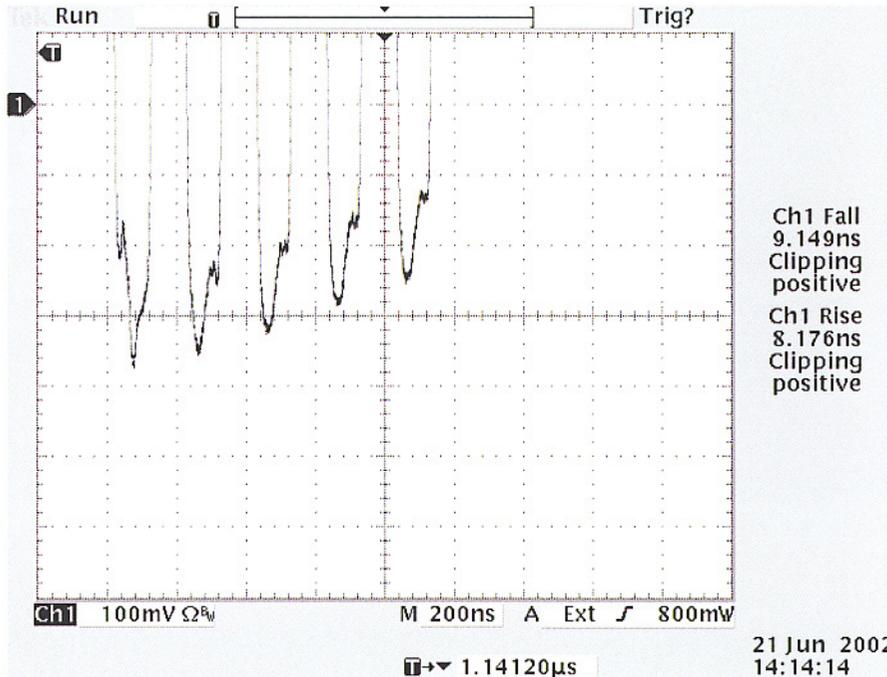
5-Pulse, 5MHz Burst @ 10 kV/div



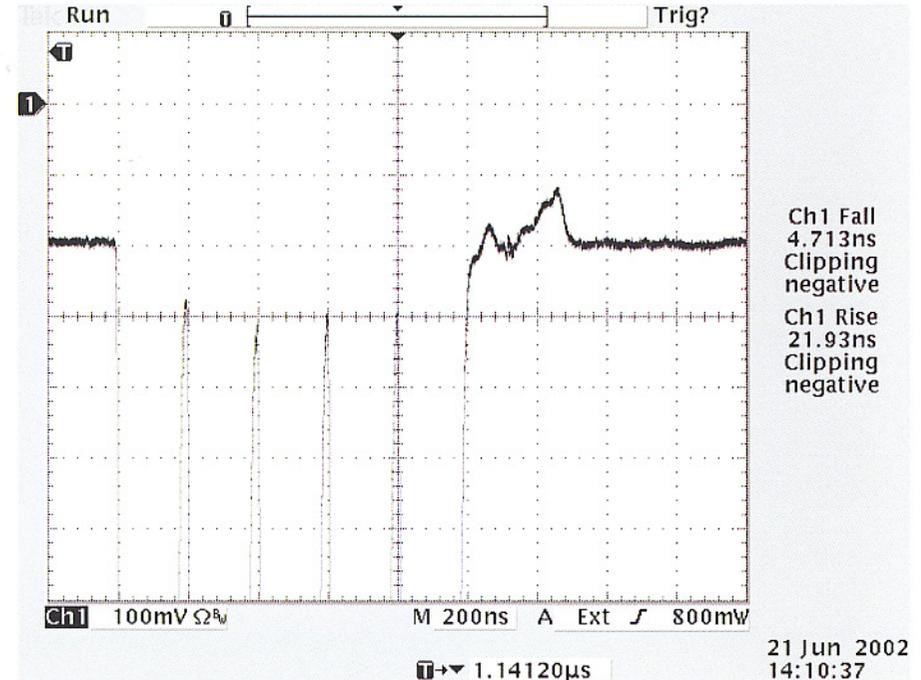
2nd Pulse of 5MHz Burst @ 1kV/div (2%/div)



# Voltage Flattop and Intra-Pulse Voltage: 50kV, 5MHz Burst



Voltage Flattop



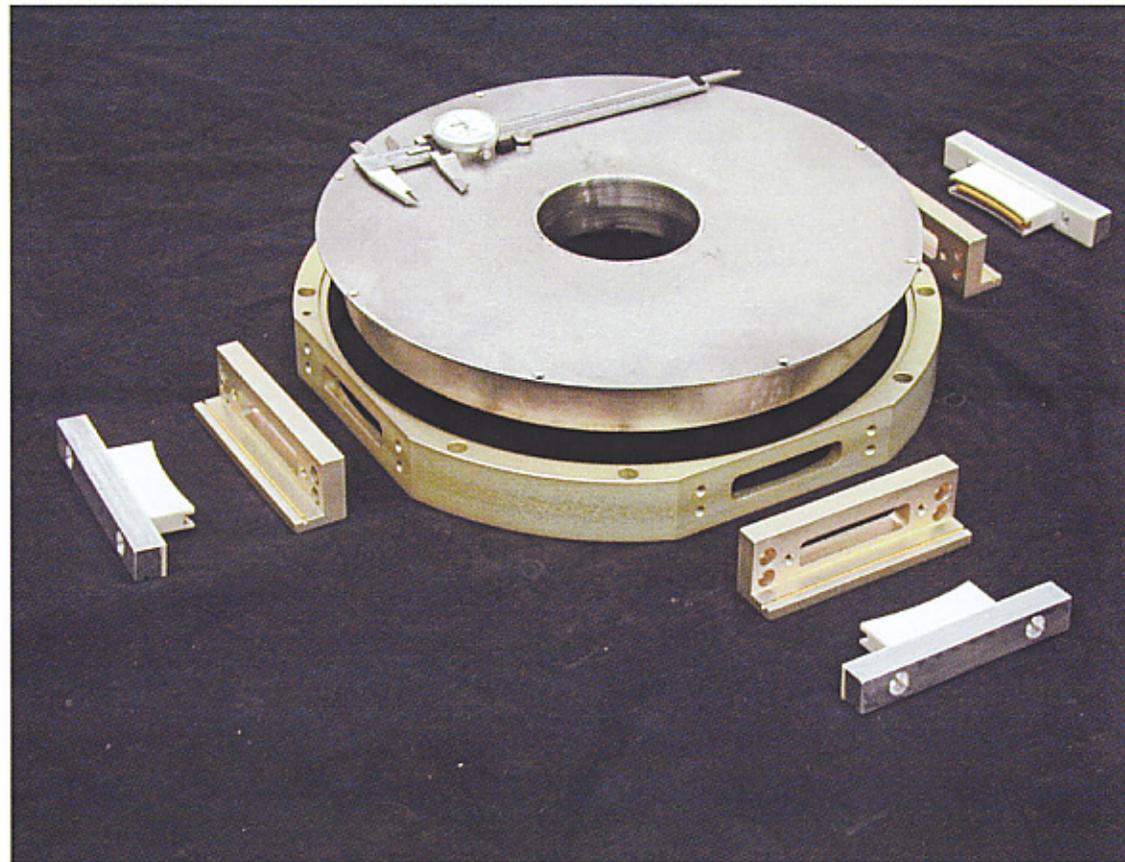
Intra-Pulse Voltage

Load Voltage @ 1kV/div or 2% / div



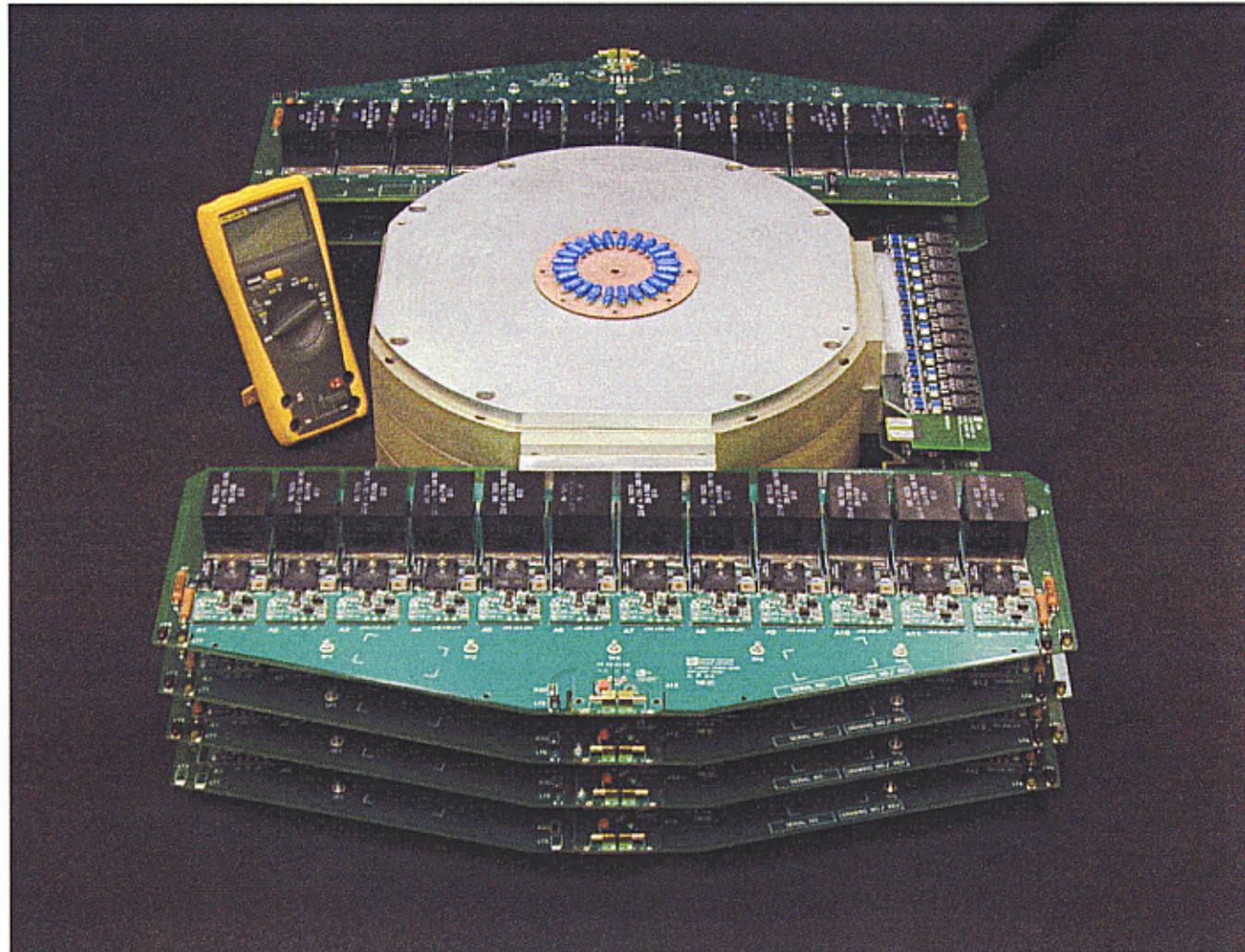


## Full Scale Adder Cell



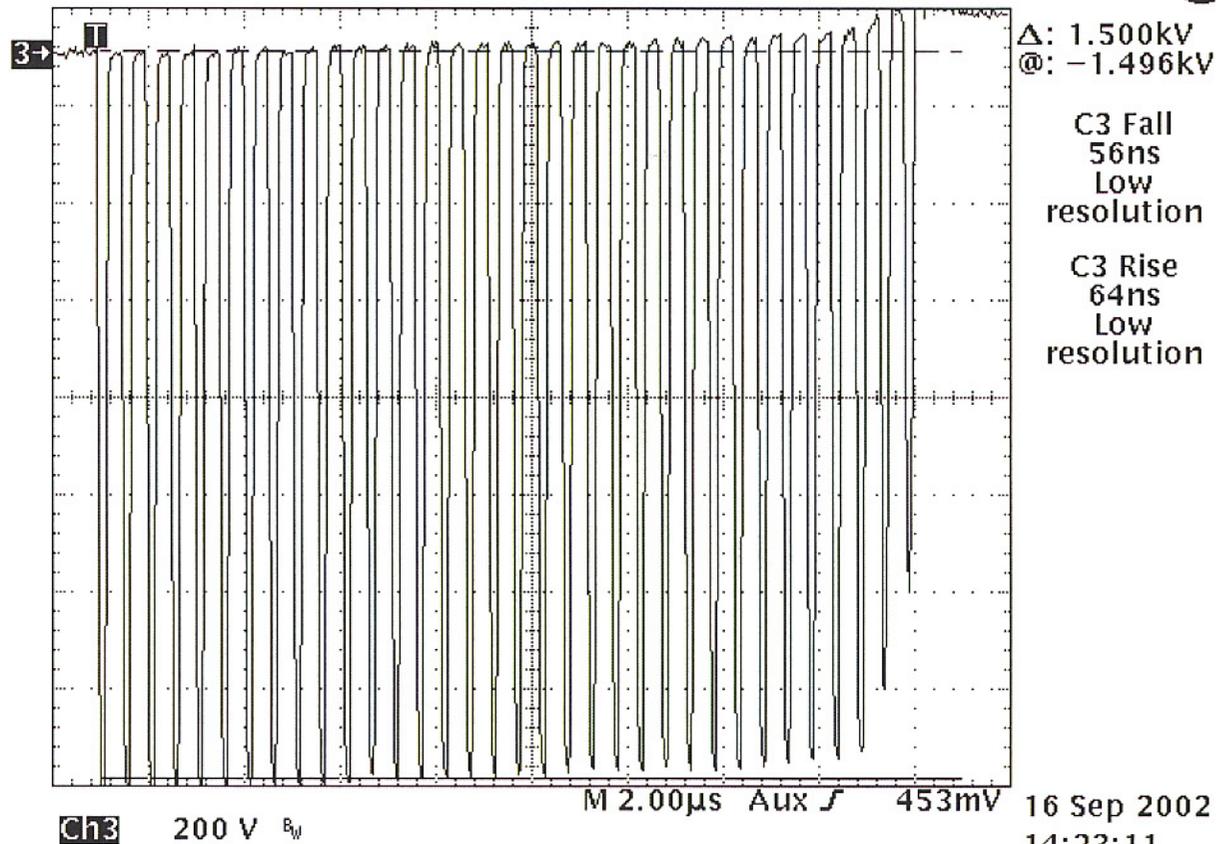
**Adder Cell Designed to Meet 24 Pulse Burst Requirement  
Shown with Feed-through Connectors**

# 4 Cell Adder Stack with Drive Boards



# Volt-second and Voltage Droop Measurements on Adder Modules - 750 Volts/Cell (2 Cells)

Tek Run: 25.0MS/s Sample 11192

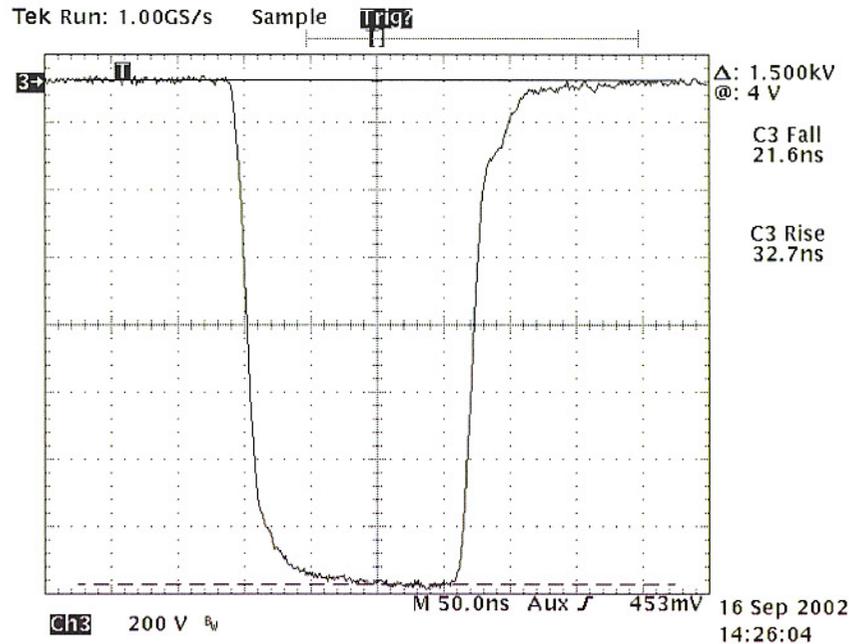


34 Pulse Burst - ~ 150 ns Pulse Width with Reset

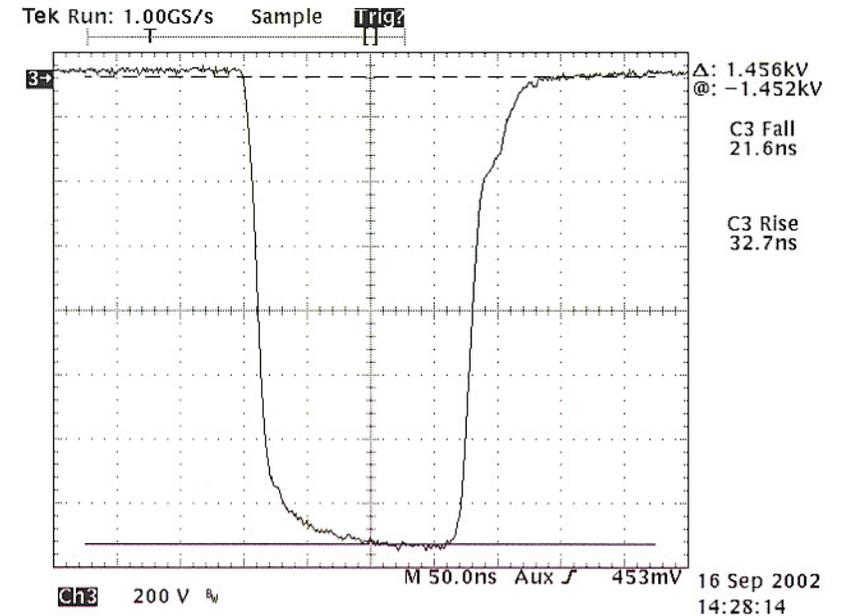


# Voltage Droop Measurements on Adder Modules

## $V_{out}$ (2 cells) on $2.125 \Omega$ Load - with Reset



1st Pulse of 34 Pulse Burst



20th Pulse of 34 Pulse Burst

Voltage Droop  $\sim 44\text{V}/1516\text{V} = 2.9\%$  over 20 Pulses.



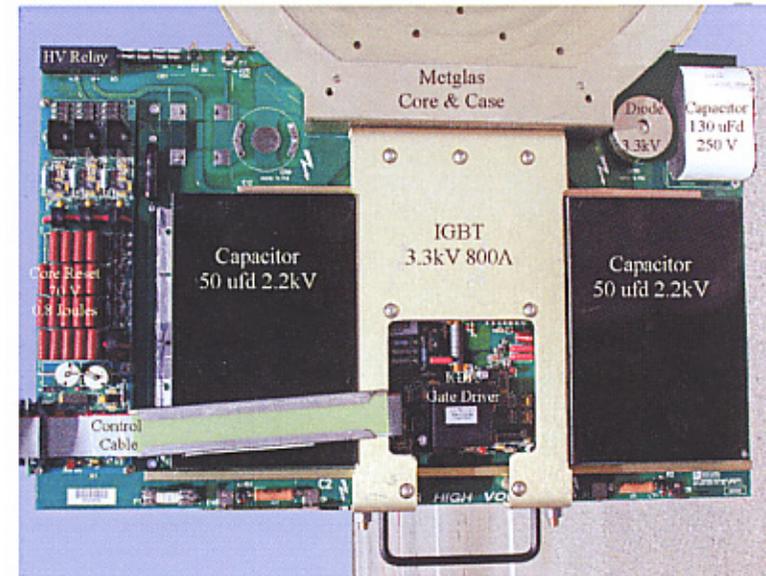
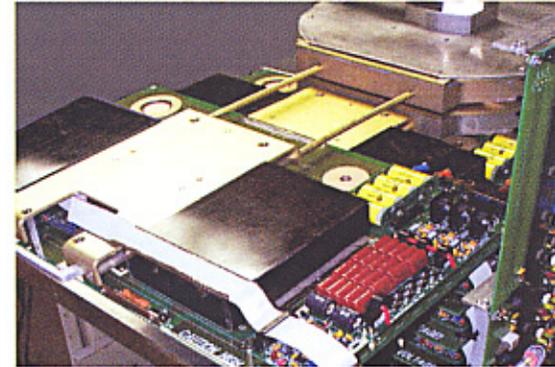
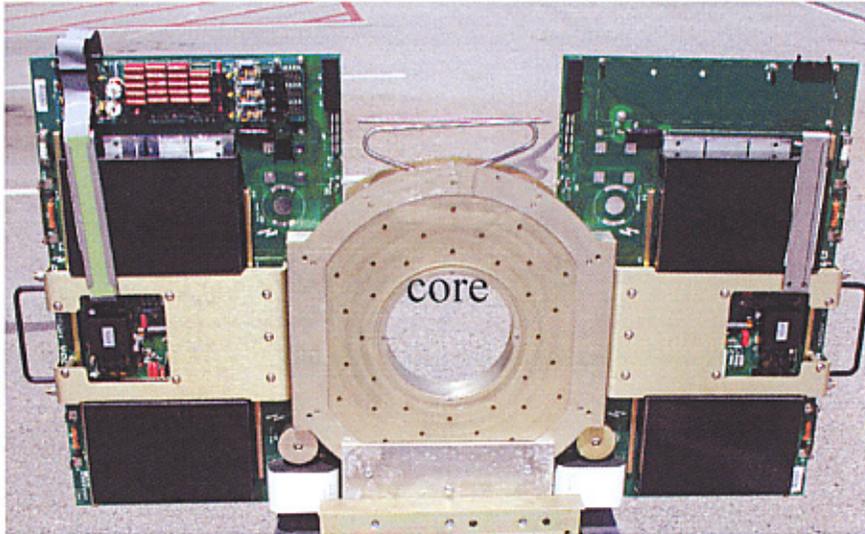
# NLC - Collaboration with SLAC for Klystron Modulator Development

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- Modulator Requirements:
  - Output Voltage 500kV @ 2kA
  - Pulse-width - 3 $\mu$ s
  - Klystron Efficiency > 80% (rise & fall times less than 400 ns)
  - Repetition Rate - 120 Hz (500kW Average)
  - Lifetime - 30 years
  - Cost < 200k\$/ Modulator



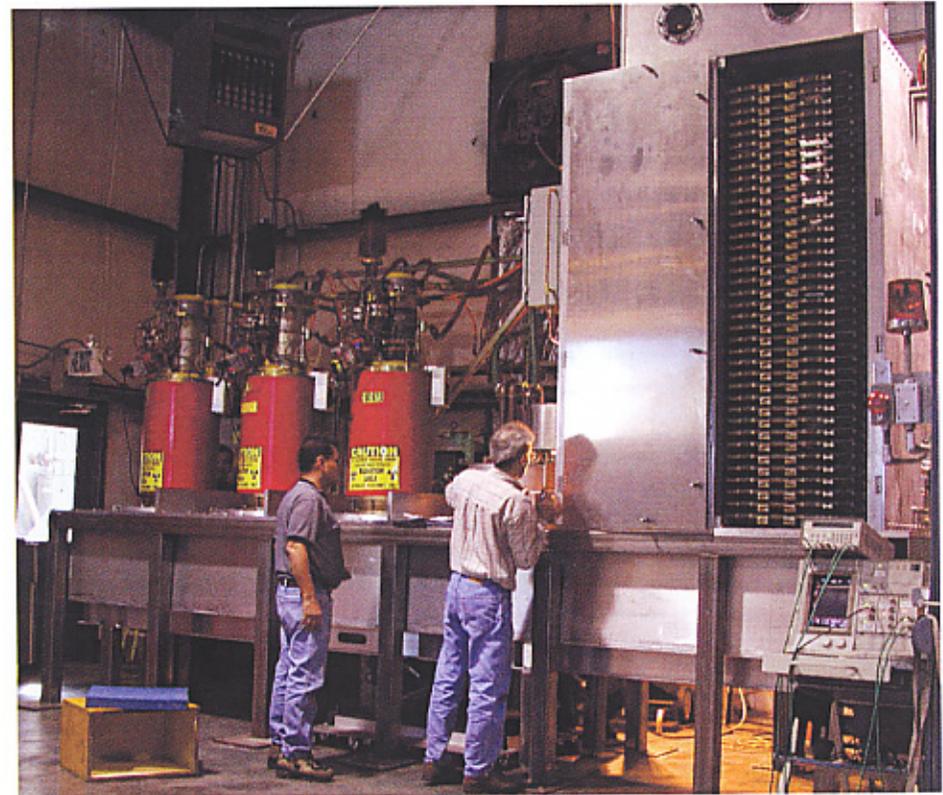
# IGBT Drivers and Core



# Prototype Solid State Induction Modulator

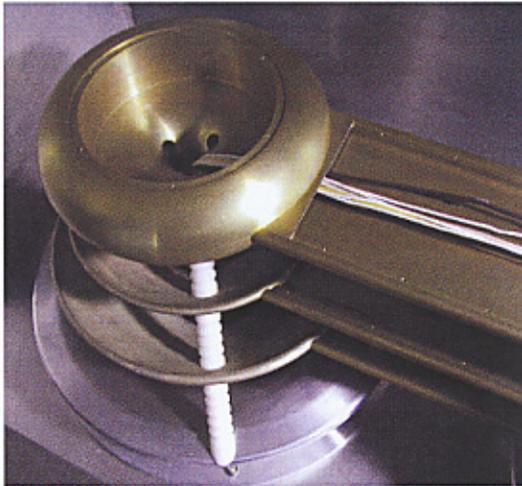


**3 turn Secondary with water load**

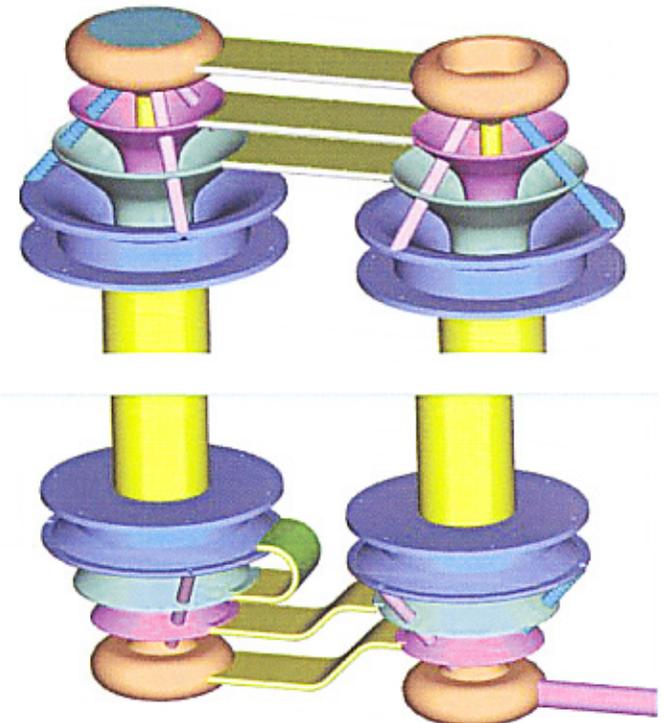


**With oil tank installed**

# Prototype Solid State Induction Modulator

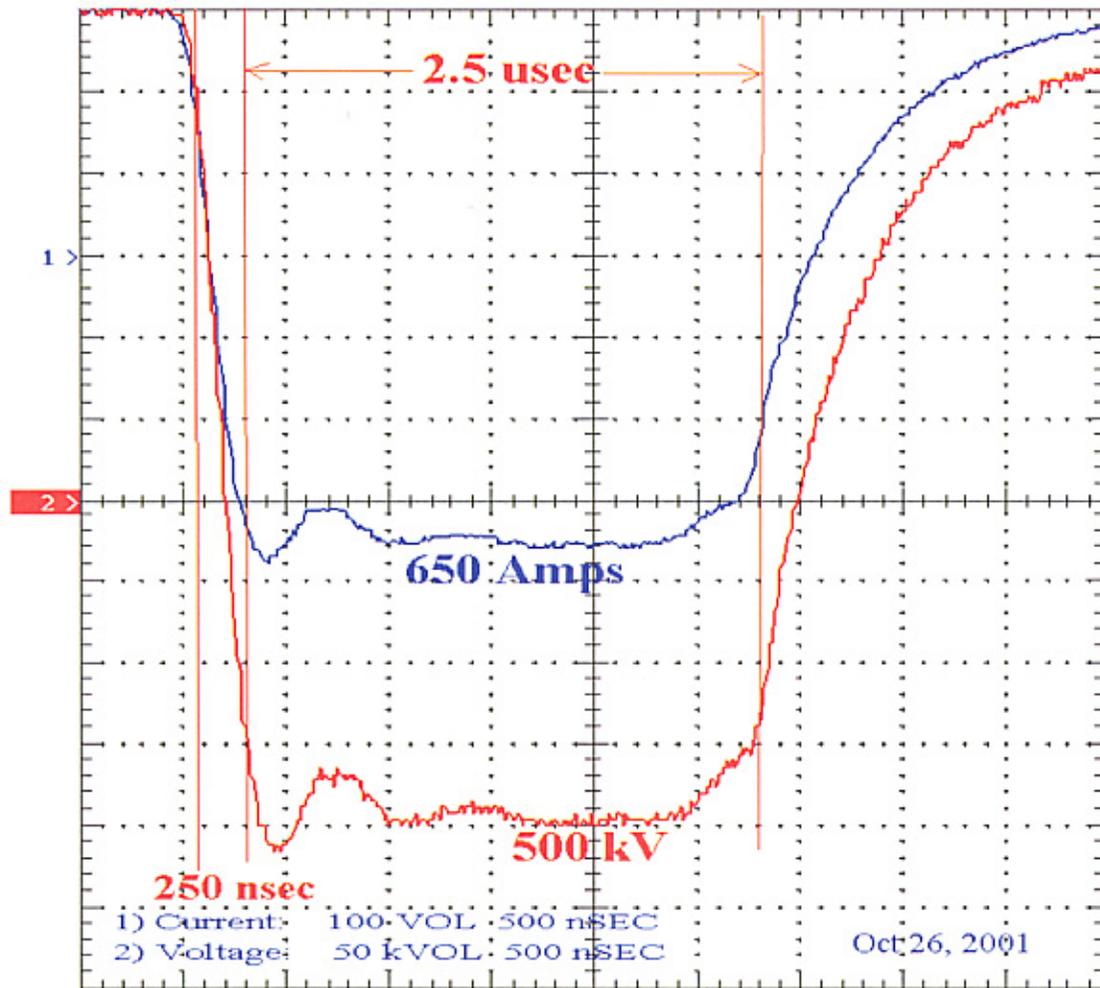


- Coaxial  
Three Turn  
Secondary  
End  
Connection



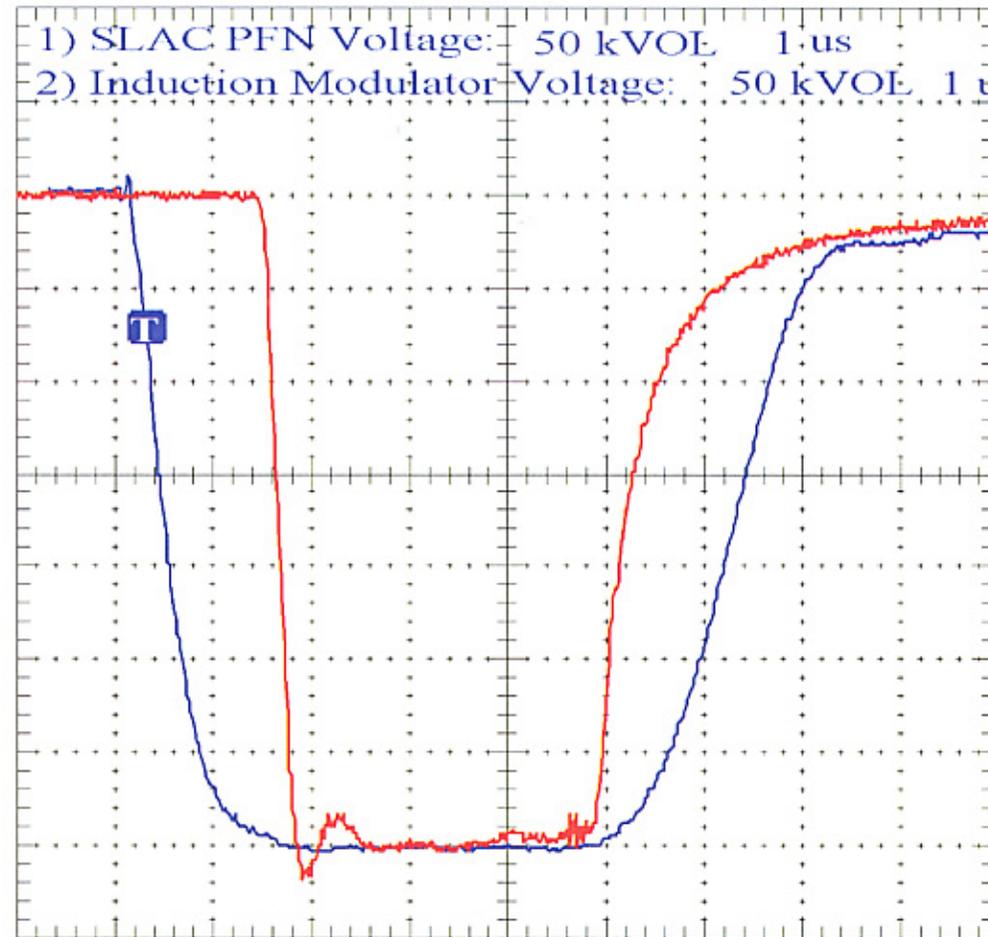
# Prototype Induction Modulator Pulse into Water Load

Three Turn Secondary  
 76 Metglas cores  
 152 IGBT Drivers



# Comparison: Induction Modulator Pulse with PFN 5045 Klystrons Pulse Voltage

350 kV, 3.0 usec  
 375 Amps PFN  
 750 amps Induction  
 Modulator waveform  
 efficiency ~89%  
 Overall efficiency  
 >80%

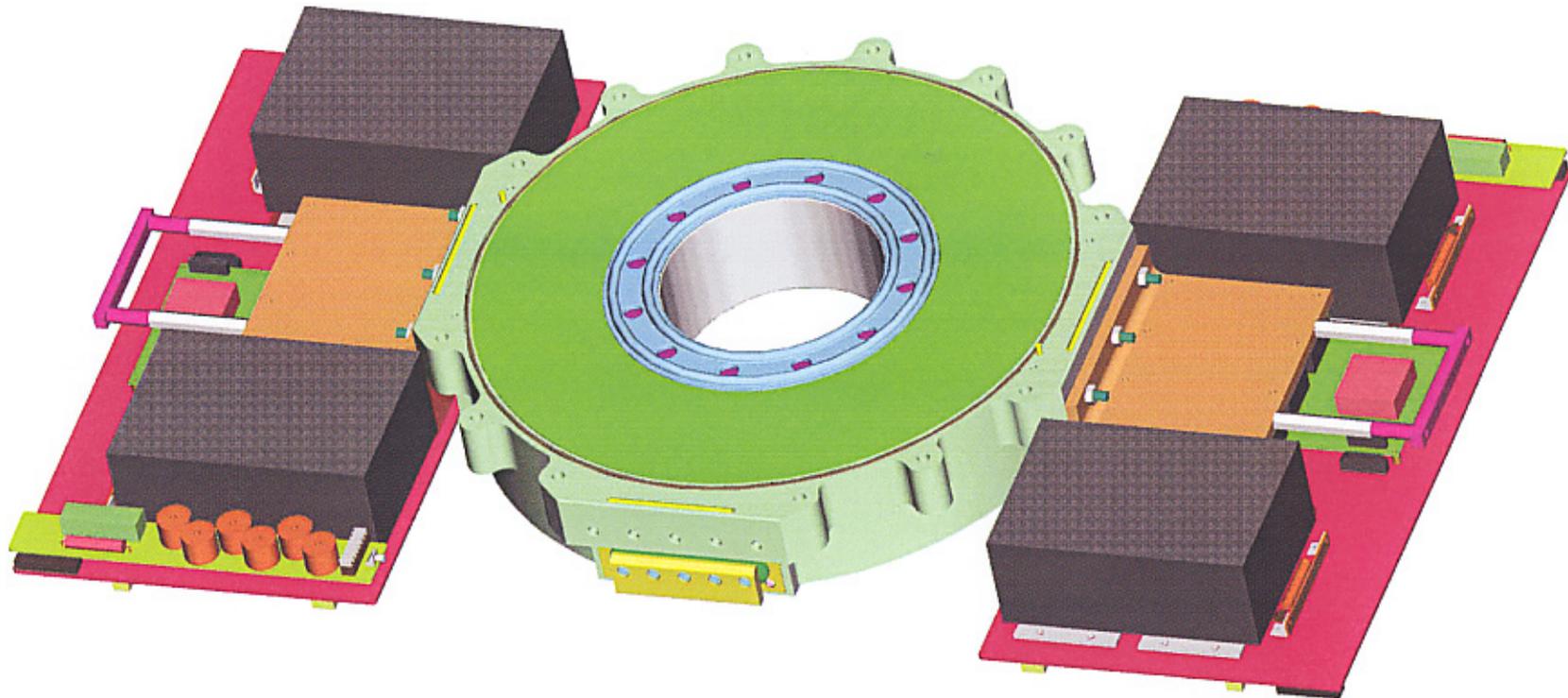


NLC - The Next



NLC - The Next Linear Collider Project

# Production Adder Cell and Drive Boards



## Summary

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- Solid-state pulsers (based on modular adder circuit topology) have demonstrated the capability of satisfying fast kicker requirements
- Solid-state adder pulsers are also capable of meeting the needs of very high peak power and high average power applications.

