Development of SiC Power MOSFETs with Low On-resistance

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Device&Process Team 1 Leader
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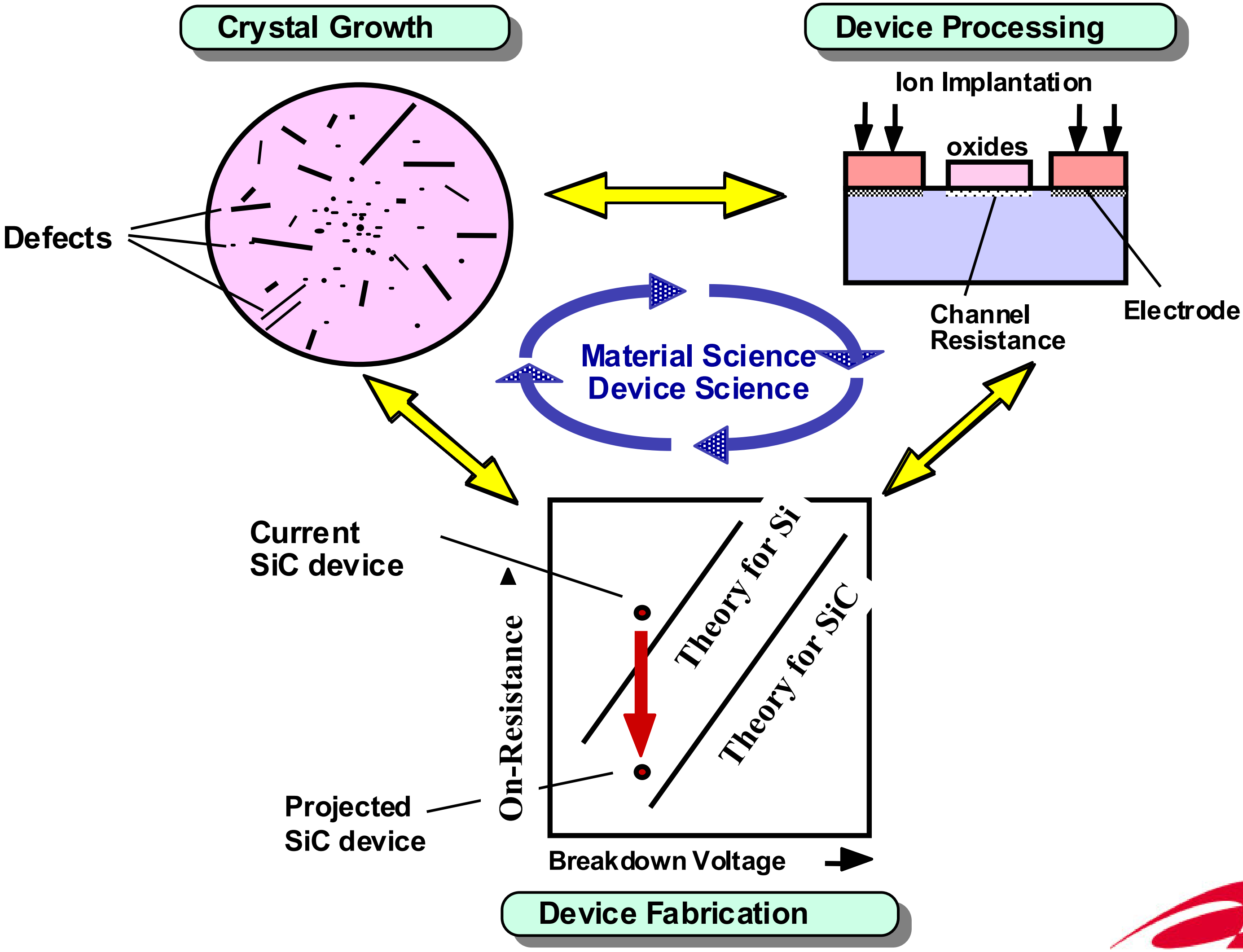
Ultra low loss Power Devices Technology Japanese National project(1998-2002)



Outline

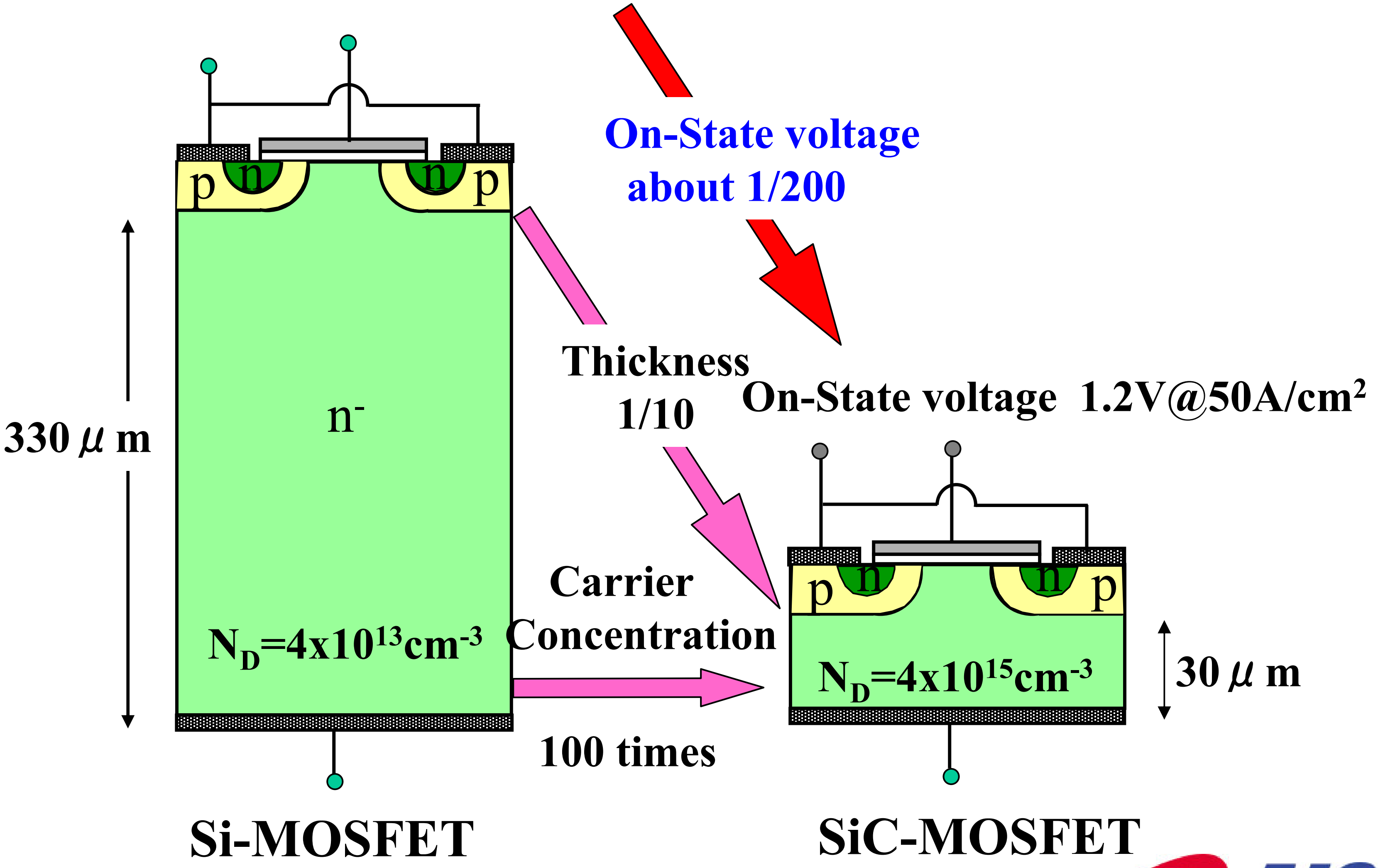
1. Background
2. Present state of SiC devices
3. Problem & Solution of SiC MOSFETs
4. Gate oxide reliability
5. Summary

Physical properties of wide gap semiconductors

Semi-conductors	Eg(eV)	Mobility (cm^2/Vs)	Saturation velocity(cm/s)	Dielectric Breakdown field(V/cm)	Thermal conductivity (W/cm・K)
3C-SiC	2.23	1000	2.7×10^7	—	4.5
4H-SiC	3.26	900	2×10^7	3×10^6	4.5
6H-SiC	2.93	500	2×10^7	3×10^6	4.5
Si	1.11	1350	1×10^7	3×10^5	1.5
GaAs	1.43	8000	2×10^7	4×10^5	0.5

SiC vs. Si (3300V MOSFET)

On-State voltage 250V@50A/cm^2



High temperature operation

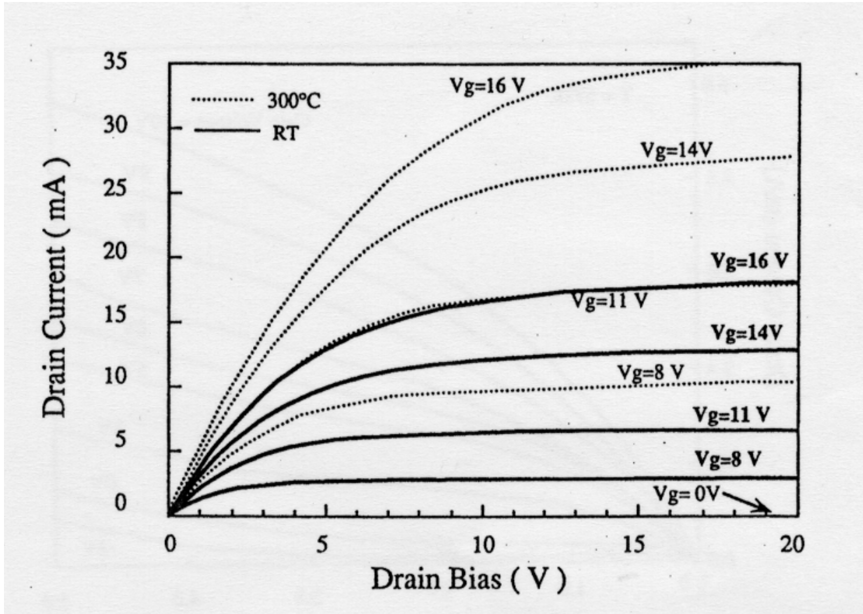
SiC

1. High thermal conductivity

2. Wide energy gap

1. High temperature operation is possible.

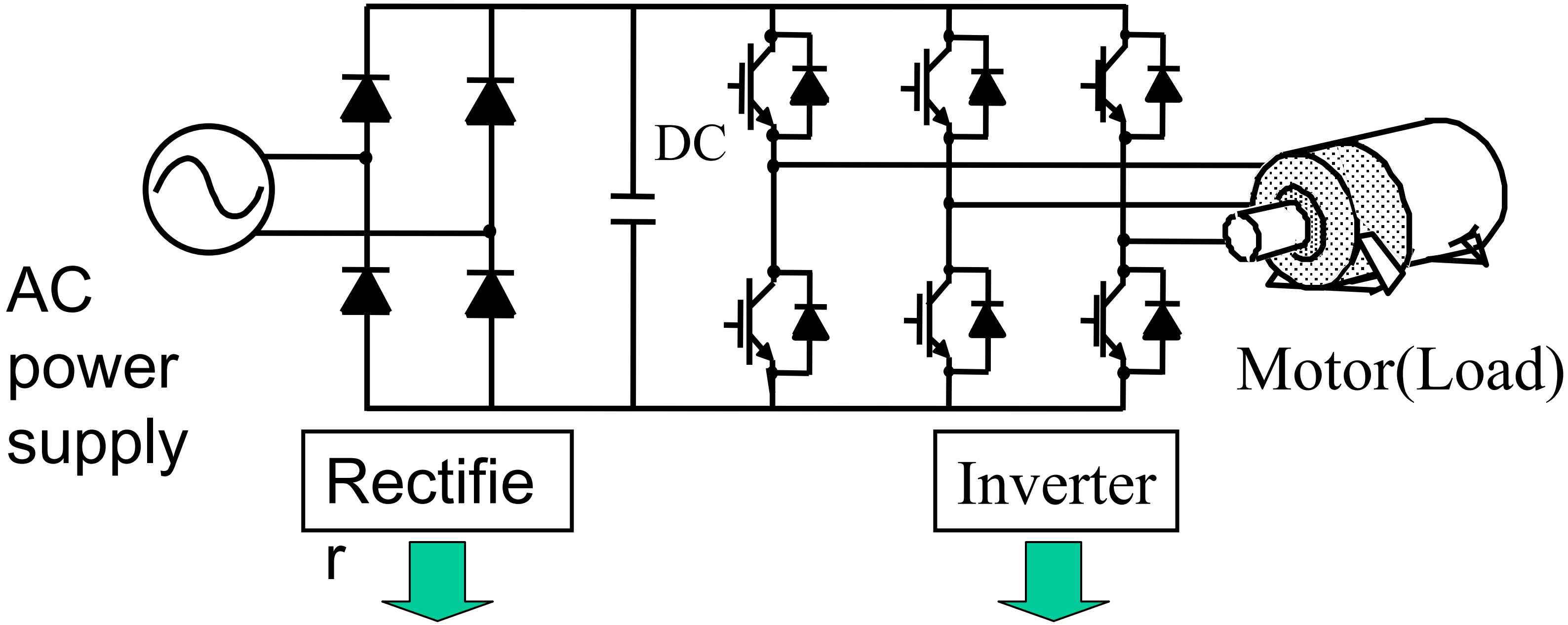
→ Powerful advantage



6H-SiC MOSFET at 300℃
J.W. Palmour et al.
Physica B,185,461(1993)

Present state of SiC devices

power electronics apparatus



Diode

- **SBD**

(Schottky Barrier Diodes)

- **PiN Diode**

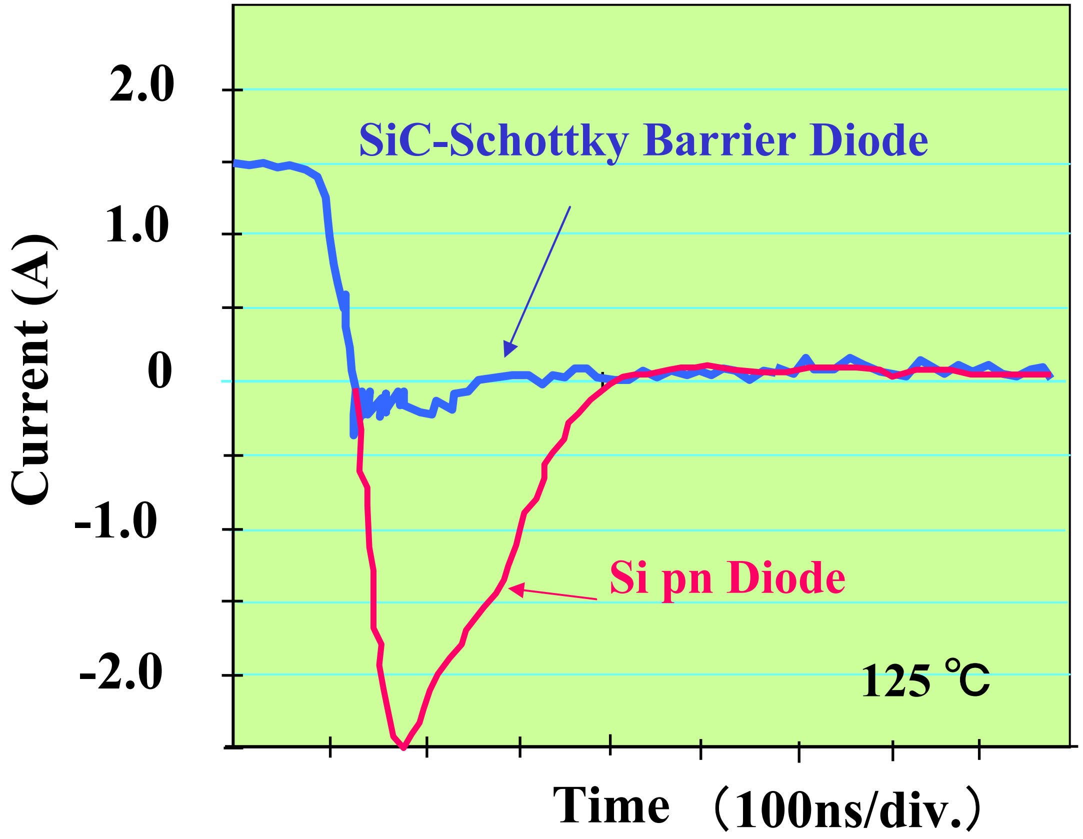
Switching Devices

- **JFET**

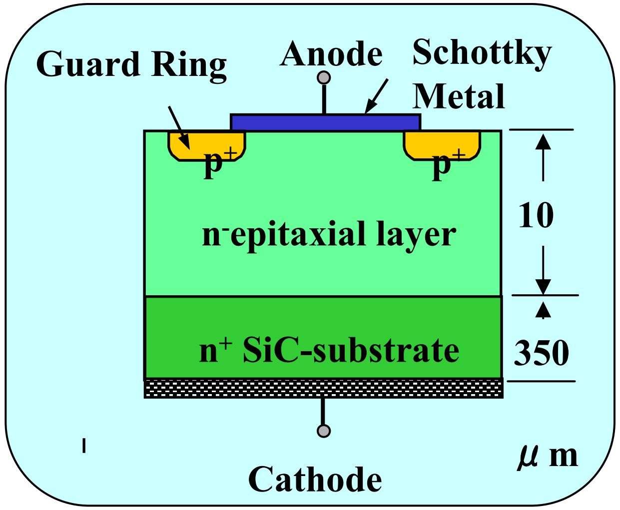
(Junction FET)

- **MOSFET**

SiC-Schottky Barrier Diodes



Reverse Recovery Characteristics



Ron :1 mΩcm^2,V_{bd}=1kV
SiCED(Siemens/Infineon)
→ Sale($3/chip)

Disadvantage of SiC JFET

SiC JFET(SIT) is nomally-on device.

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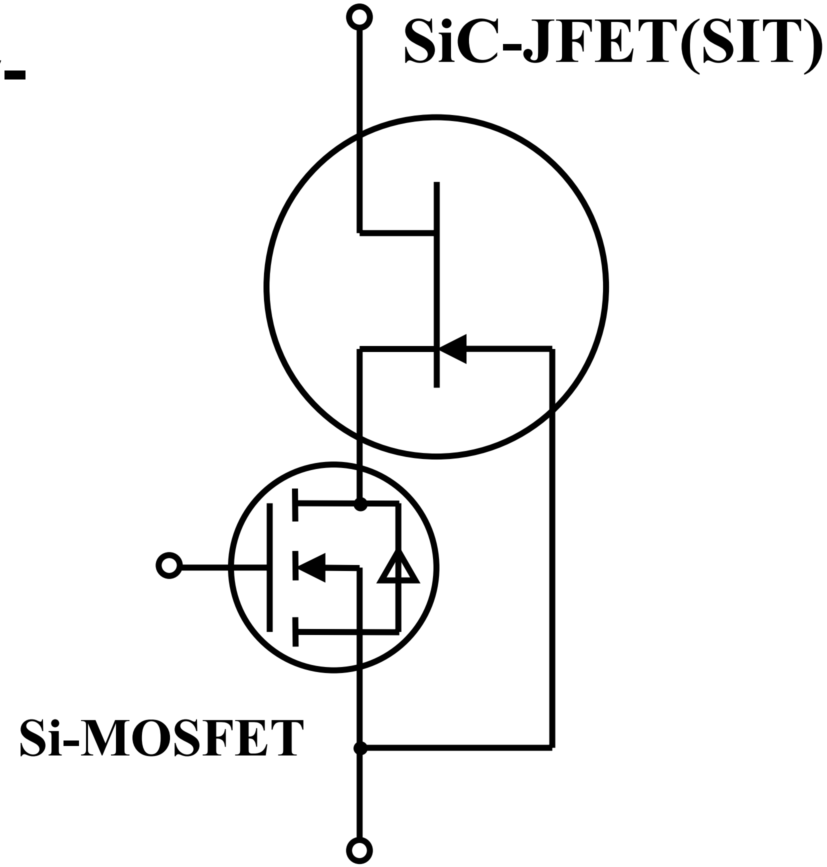
SiC-JFET Cascode Arrangement with Si-MOSFET is necessary.

⇩

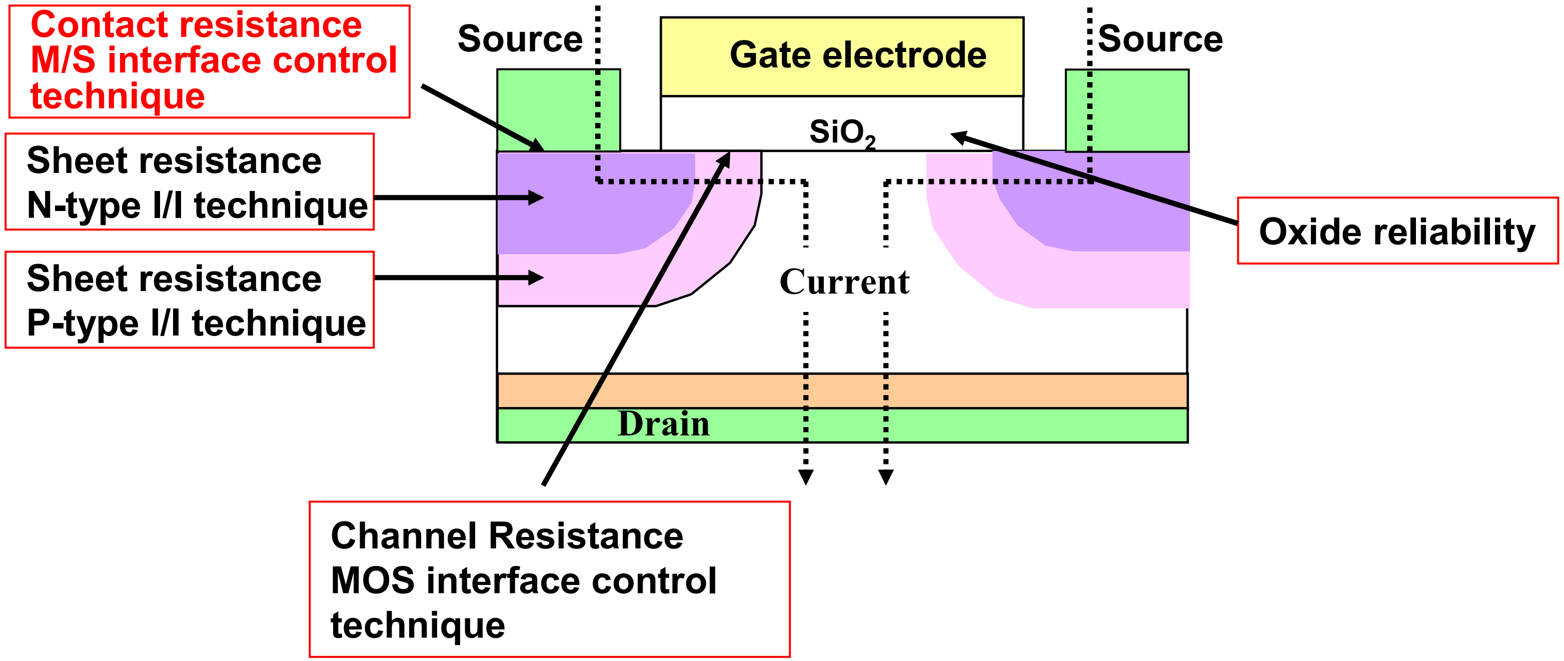
SiC MOSFET is ideal because it is normally-off type device.



By P. Friedrich et al;"Static and Dynamic Characteristics of 4H-SiC JFETs Designed for Different Blocking Categories", Mate.Sci. Forum 338-342,2000,p.1243-1:

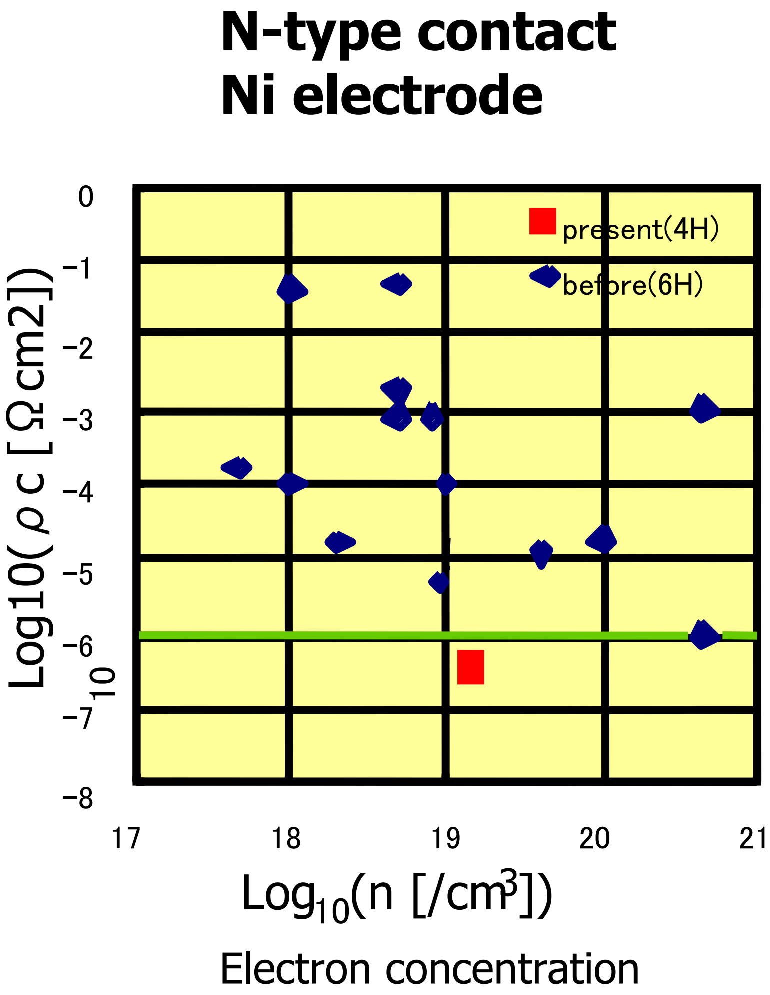
Problems of SiC MOSFETs

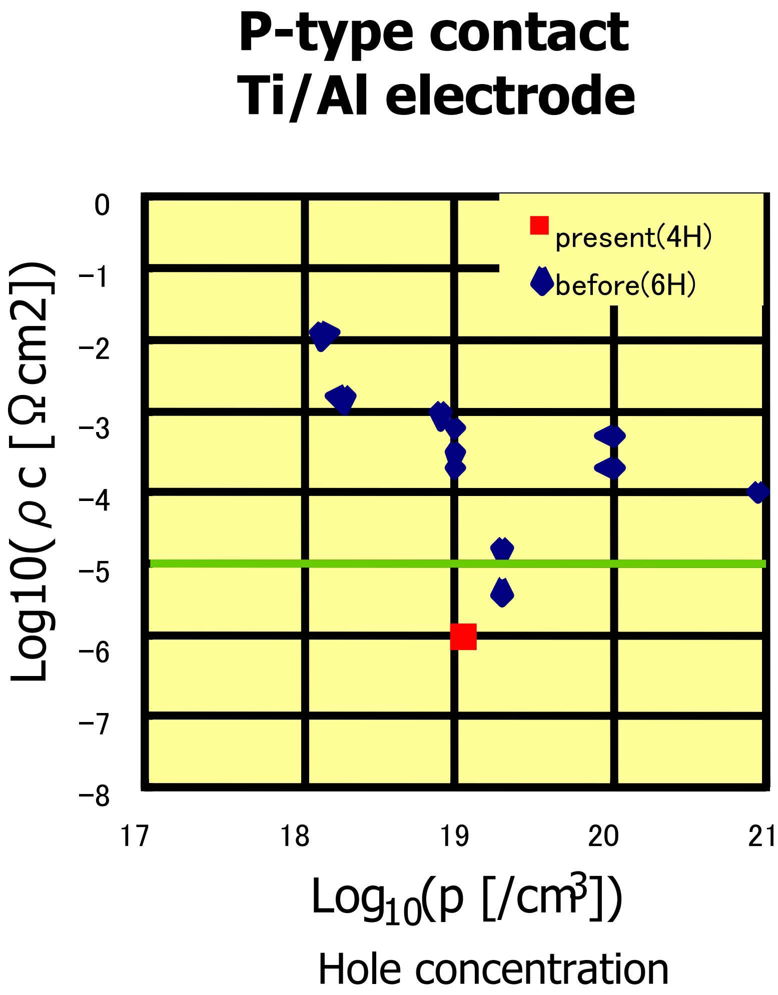
1. High Ron＝Contact +Sheet +Channel



2. Oxide reliability

Comparison with before data

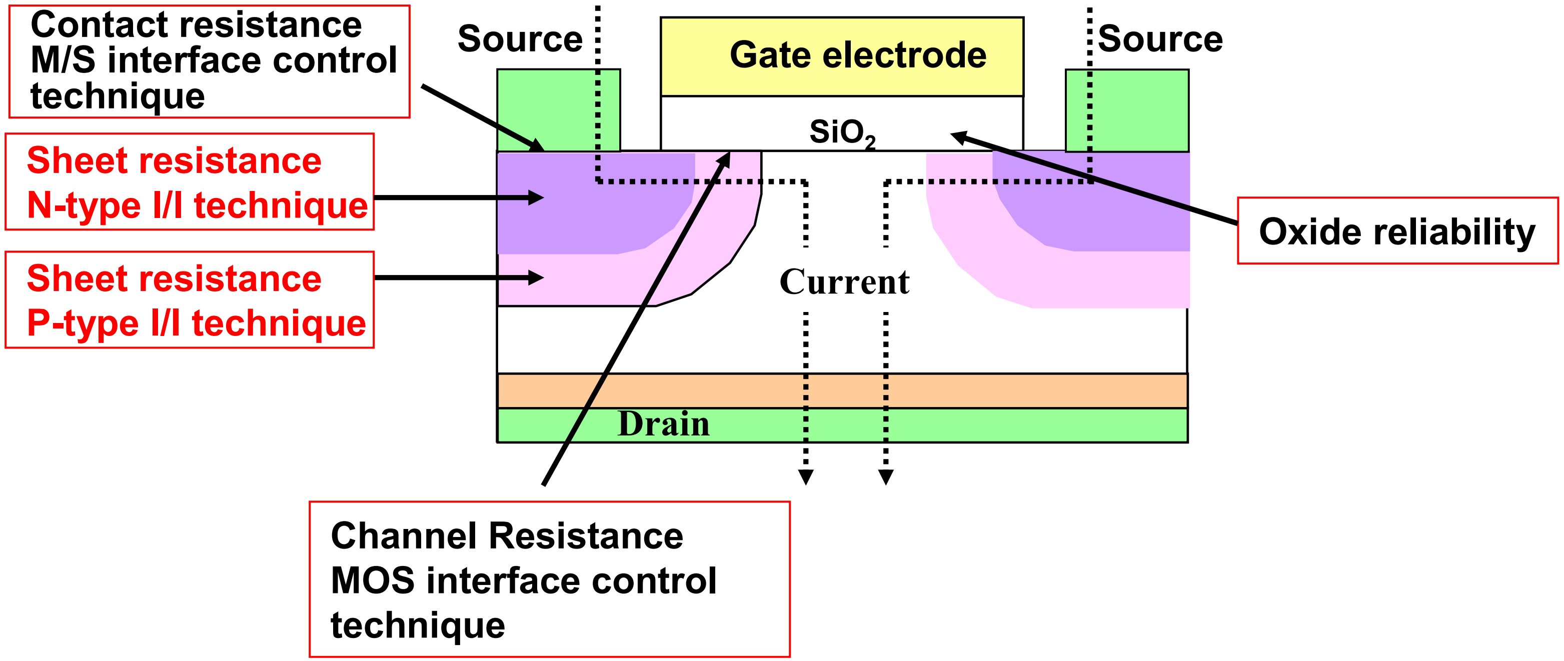




"Crofton *et al.*, Phys. Stat. Sol., **202** , 581 (1997)."

Problems of SiC MOSFETs

1. High Ron＝Contact +Sheet +Channel



2. Oxide reliability

Reason of high sheet resistance

Very High temperature >1500℃and long annealing is necessary for impurity activation.

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Impurities disappear with Si from SiC surface

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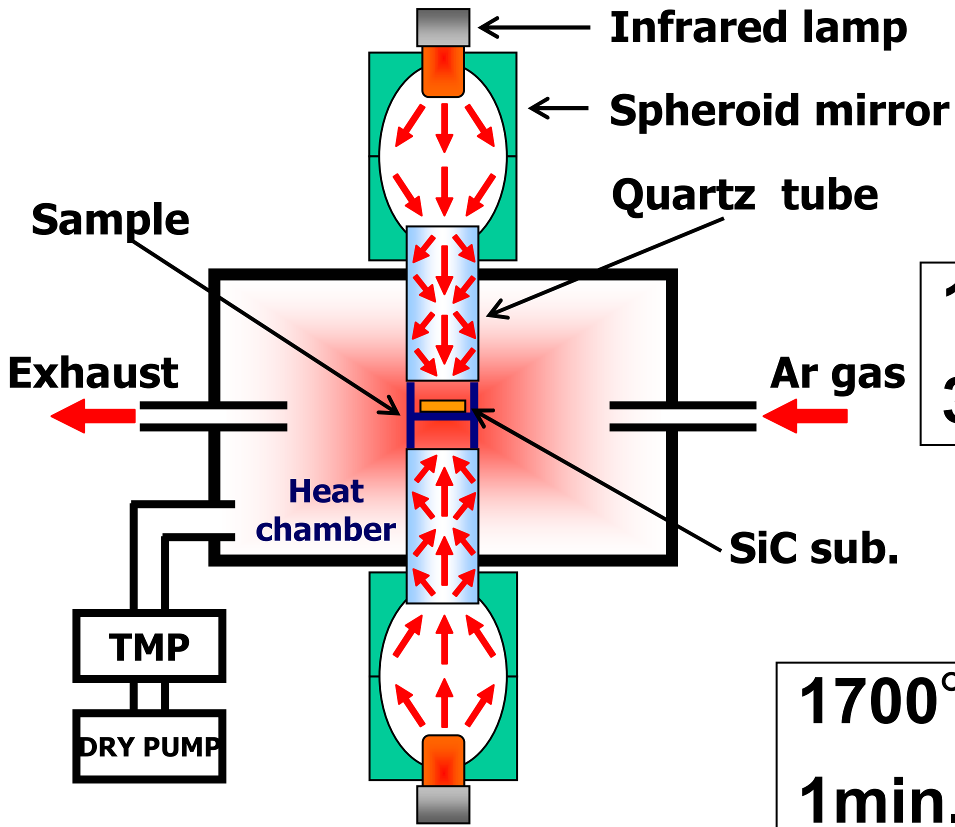
Very high sheet resistance

Super fast and high-temperature activation annealing equipment

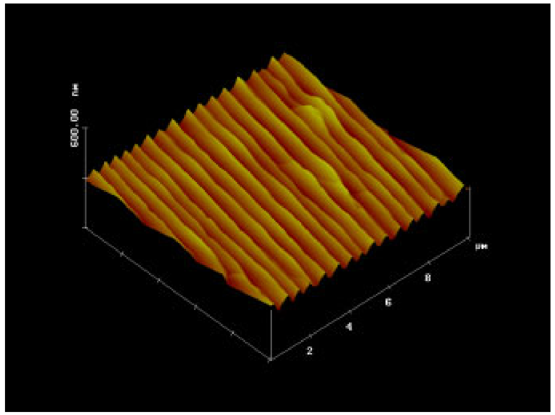


Concept of equipment

SiC surface

1700℃

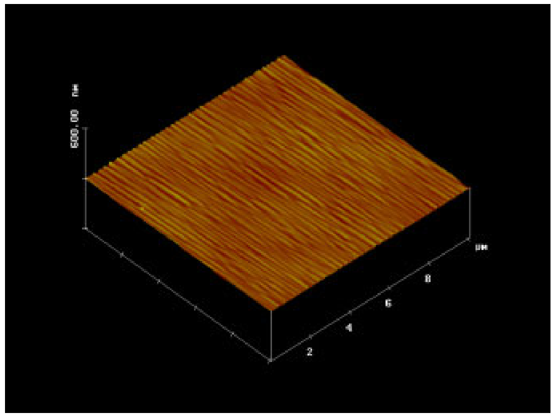
30min.



1700℃

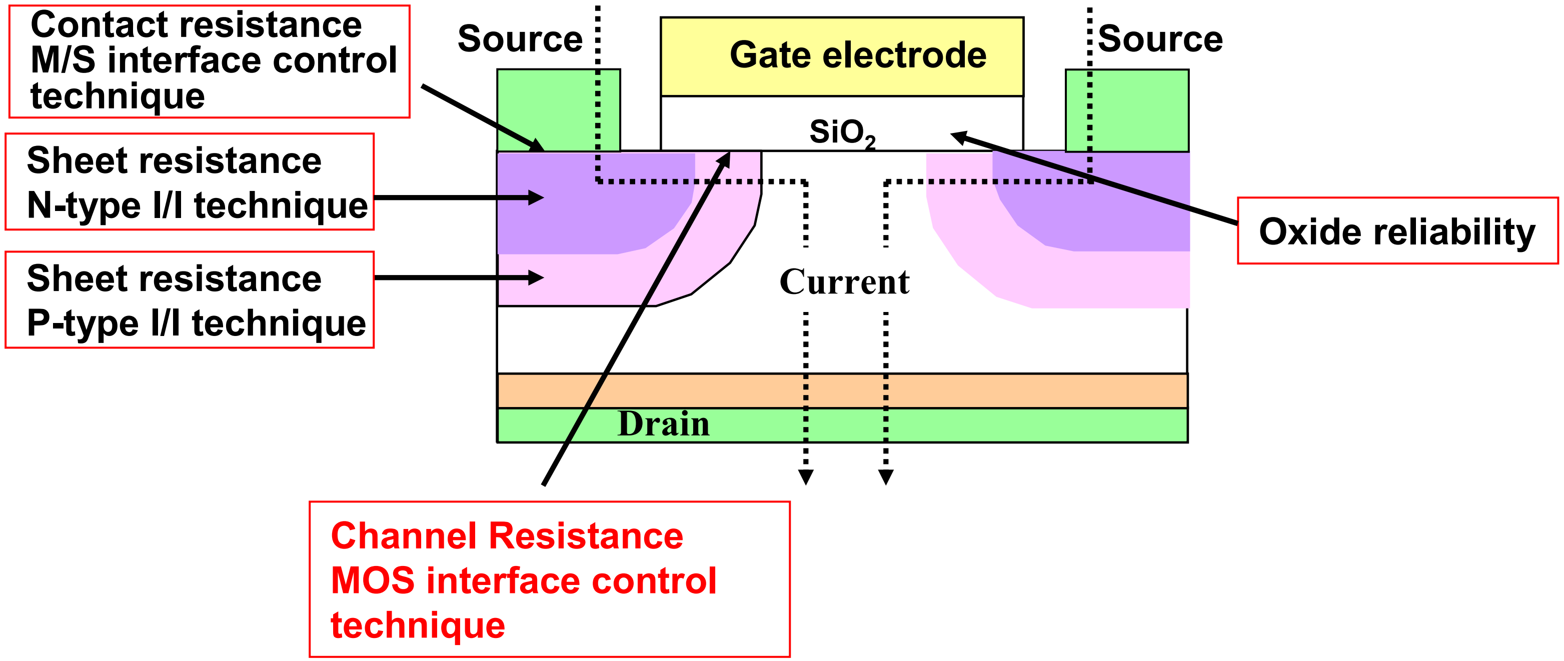
1min.

Rs=38Ω/□



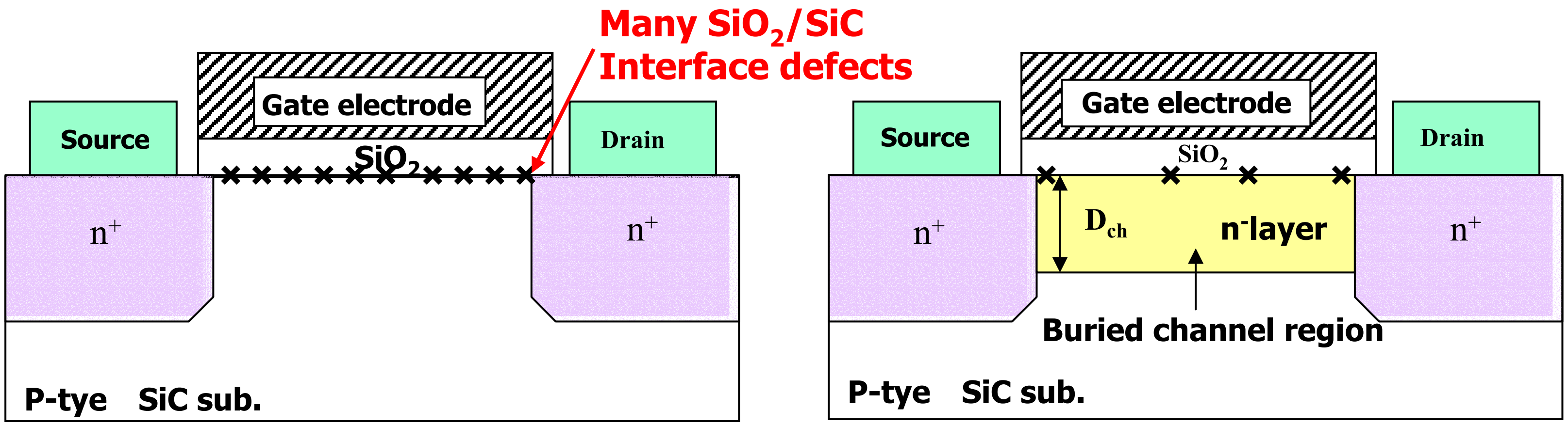
Problems of SiC MOSFETs

1. High Ron＝Contact +Sheet +Channel



2. Oxide reliability

Reason of high channel resistance



SiO_2/SiC interface

⇩

Large amount of interface defects

⇩

Low channel mobility

⇩

High channel resistance

Our results

MOS interface control

1. Dry oxidation+wet re-oxidation
2. Buried channel structure

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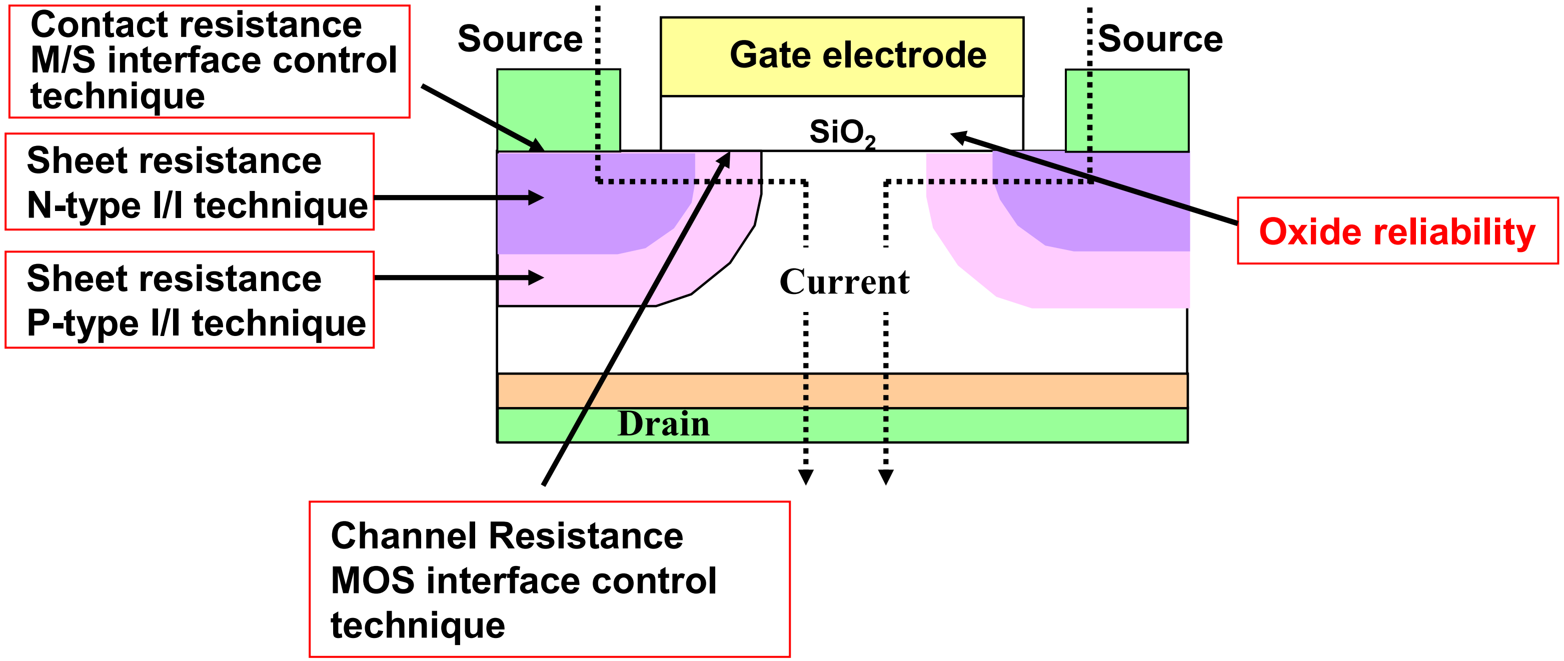
μ_{FE} > 200cm²/Vs is achieved.

Problems of SiC MOSFETs

1. High Ron＝Contact +Sheet +Channel



2. Oxide reliability

Problem of Oxide reliability

1. Energy barrier height is small.

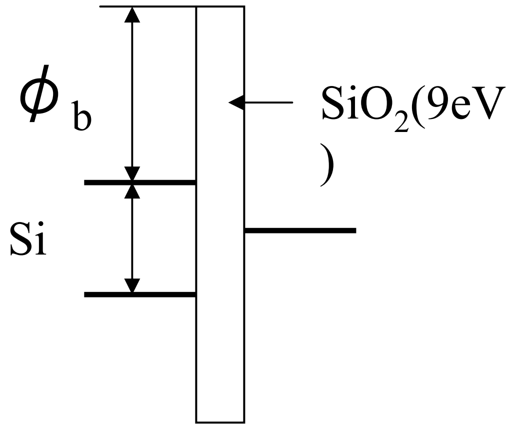
Electron injection into SiC oxide is easier than that of Si.

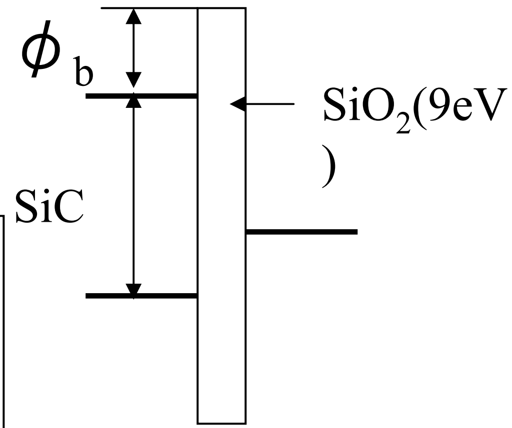
2. Carbon reminds in SiO_2 film.

Residual carbon causes large leak current.

3. Working temperature of SiC is expected to be higher than that of Si.

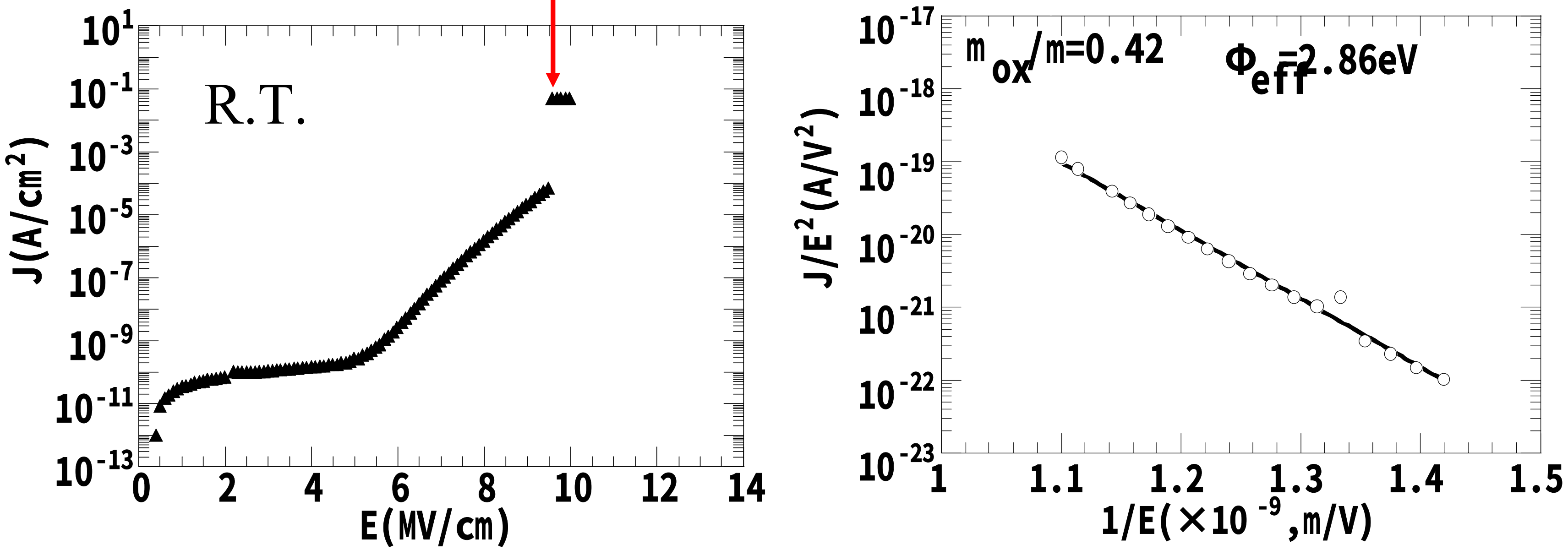
Circumstance of SiC oxide is harsh.





Current VS. Gate voltage

9.5MV/cm(This is same as Si MOS)



Long time reliability at high temperature is important. → Data is insufficient.

Summary

1. SiC JFET

Ron=70mΩcm^2、Vbd=2000V

Normally-on、Cascode arrangement is necessary.

→ MOSFET is ideal device.

2. SiC MOSFET

(1) Contact and Sheet Resistance is sufficient low.

(2) MOS interface control technique

- μFE of 216cm^2/Vs was achieved.
- Lateral resurf MOSFET

Ron=51mΩcm^2、Vbd=630V

Dynamics characteristics: rise time=20ns, fall time=15ns

- DIMOSFET

Ron might decrease below 10mΩcm^2, I am investigating now it.

- Oxide reliability at high temperature is left-behind.

I am investigating now it,too.