A PC-based Single-Bunch Current Measurement System for PETRA

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Abstract

PETRAII has been operating since spring 1996 with a new control system, based entirely on PC hard- and software. The core of the *bunch current measurement* is a commercially available ISA PC-board, equipped with a 12-bit ADC for the data acquisition and 64 kByte memory. Application program structure and features, as well as first operational experience with this prototype are reported. As this *current monitor* has a modular design, it will be easy to clone for the other accelerators DESYII, DORISIV, and HERA with only minor changes.

1 INTRODUCTION

The HERA e/p collider (27 GeV e^+/e^-, 820 GeV p) and the DORIS synchrotron radiation facility (4.6 GeV e^+) are currently in operation at the DESY laboratory in Hamburg, Germany. Several pre-accelerators are used to boost the particle energies to their injection energy levels.

The development of a "standard" instrument for use in most accelerators and transport-lines at DESY was one of the main goals. The constant 96-ns interbunch space (or multiples of 96 ns) in all accelerators[1] and the available bunch-trigger signals simplified our task. This type of monitor instrumentation is used in routine operation for various tasks:

- In conjunction with a *DC current monitor* it provides a measure of the "bunching" in a proton accelerator.
- Measurement of the transfer efficiency between accelerators and through transport-lines.
- "Timing" calibration and matching in and between accelerators, i.e. the reference ("first") bunch in relation to the rf-bucket based marker systems (PIT, HIT).
- Other calibration purposes, e.g. background and specific luminosity counting, in HEP experiments.

PETRAII is used to boost the particle energies of p and e^-/e^+ for their injection into HERA and also serves now as a synchrotron light source. In association with PETRA's new *control system* [1] a new PC-based bunch current measurement system has been developed. The main (hardware) components are shown in the block-diagram (Fig. 1).

[1]Except LINACIII and DESYIII, which run with protons at lower energies.

Pickup The *inductive pickup* [2], [3] acts as the secondary winding of a transformer and returns a pulsed signal proportional to the charge in a bunch $\equiv$ *bunch intensisty*.

Analogue electronics The pickup signal is processed with filter-, amplifier- and track-and-hold techniques before digitization by an analog-to-digital converter (ADC).

Trigger electronics supply the ADC and the track-and-hold amplifier with bunch-synchronous trigger signals.

Server-PC hardware The hardware of this *server-PC* includes the commercial *ADC-board*, a digital *I/O board* and a *network interface board*.

Server-PC software A set of software routines is used to control the measurement system. A part of the software is supplied with the ADC-board as low level interface, other routines of the server software were written in-house.

Principle of operation

The inductive pickup in PETRA generates broadband, pulsed signals which are proportional to the bunch charge (intensity). They are spaced in multiples of 96 ns, with a maximum of 80 bunches in the 2.3 km long accelerator. A *lowpass pulseforming network*, as well as the dispersion on the rather long coaxial cable "smear" (stretch) the signals to $\approx$ 60 ns width. Because of the *AC-coupling* of the pickup a shift of the baseline has to be accepted, but helps to suppress low frequency noise and distortion signals. A switchable amplifier/attentuator section is available, but is not used so far (set to "0 dB"). A fast *track-and-hold amplifier* is needed to "freeze" the bottom and top voltages of each signal pulse. The hold-time is set to approximately 20 ns, which is sufficiently long for conversion with the buffered ADC. Two samples per bunch signal (the bottom and top) are digitized because of the AC-coupling, requiring a sampling rate of $>$ 20 Ms/s.
The signals are digitized with an ADC-board, which sits in a ISA-slot of the server-PC, and stored in the on-board memory. Up to 32 kWords (12-bit) can be sampled in a single *measurement cycle*. The data is *memory-mapped* to the PC-memory, where the difference of two consecutive words (top minus bottom) are computed. This difference

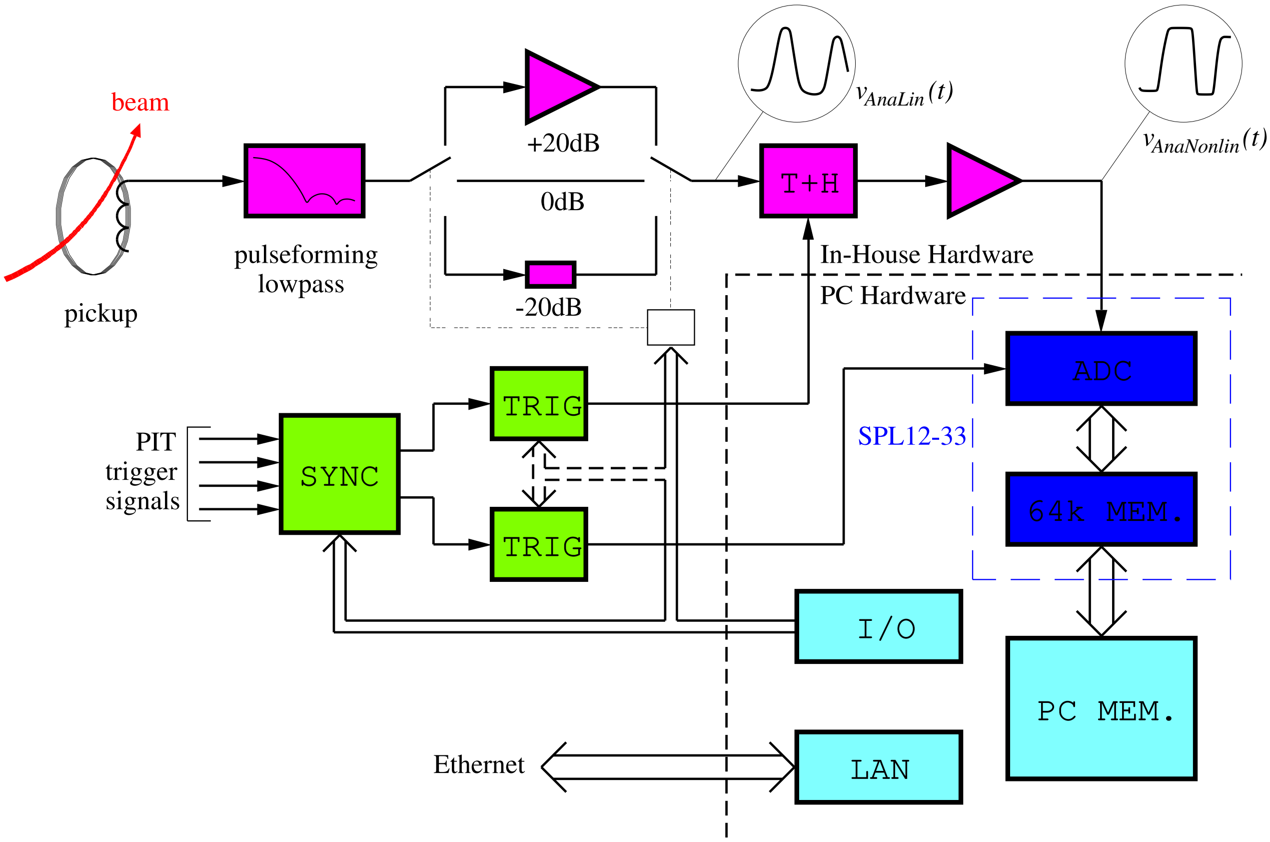

Figure 1: Schematic drawing of the hardware of the bunch current monitor.

data is converted into mA or nC and sent with other status information to the control system (LAN interface using the IPX protocol).

2 HARDWARE

The pickup and the analog signal processing, up to the input of the ADC-board, was developed completely at DESY. Also the trigger signal processing was realized in-house. The analog-to-digital signal conversion and subsequent digital data processing, storage and transmission are based on a commercial PC with several ISA plug-in boards.

Analog Signal Processing

The response of the linear analog sections to a p- or an e^-/e^+-bunch is defined mainly by the transfer characteristics of the pulse-forming low-pass filter; it is designed to have the lowest upper frequency limit ω_{LP} in the signal processing chain. As the bunched particles excite much higher frequencies, $\omega_{\mathrm{bunch}} \gg \omega_{\mathrm{LP}}$, the output signal of the filter is proportional to its impulse response $h_{\mathrm{LP}}(t)$ and therefore the filter integrates over the particle charges e in the bunch:

$$\begin{aligned} v_{\mathrm{AnaLin}}(t) &\propto h_{\mathrm{LP}}(t) \\ &\propto i_{\mathrm{bunch}} = k \int_{t_{\mathrm{bunch}}} \mathrm{n}\, e\, d\tau\,. \end{aligned}$$

Thus the measurement of the peak value (top) of $v_{\mathrm{AnaLin}}(t)$ (at the input of the track-and-hold amp) delivers a bunch current proportional value which is independent of bunch length variations. Unfortunately the AC-coupling of the inductive pickup causes a baseline shift, whose value depends on the number of bunches and on their intensity. For this reason a second measurement has to be made of each pulse in $v_{\mathrm{AnaLin}}(t)$. It takes place prior to the detection of the top value, just before the pulse signal "starts", in this way measures the baseline between the bunch signals. The baseline-shift corrected bunch current is computed as the difference between the two successive measurements:

$$i_{\mathrm{bunch}}(n) \;=\; k\,[v_{\mathrm{top}}(n) \;-\; v_{\mathrm{bottom}}(n)]$$

Here n indicates the bunch number and k is the calibration constant of the system.

The bandwidth and the gaussian-like response function have been choosen for the low-pass so that the pulse signal at its output is as "long" as possible as well as smooth and free of ringing, but does not run into the signal-response of the following bunch. The bottom and the top values of this pulse signal are spaced by $\approx$ 35 ns. The following track-and-hold amplifier stage samples and freezes the values for 20 ns. This time of constant analog value is sufficient for the analog-to-digital conversion.

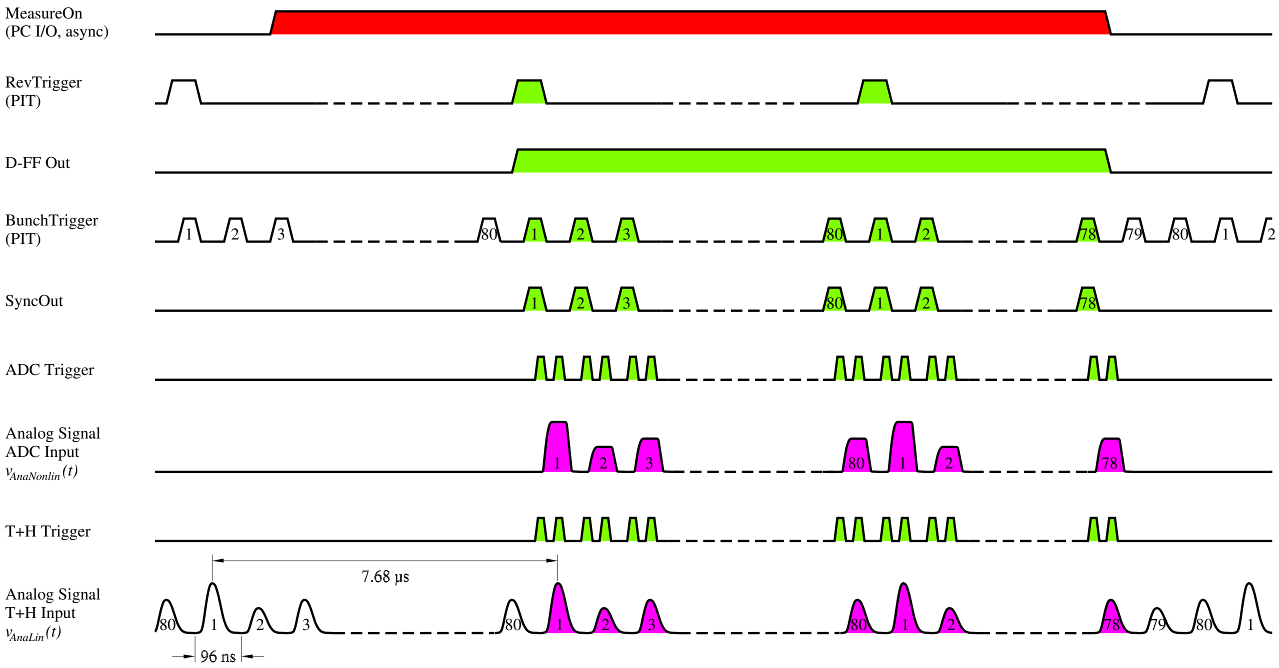

Figure 2: Timing diagram of the analog and trigger signals.

Trigger Signals

PETRA is equipped with a timing system (PETRA Integrated Timing, PIT [4]), which delivers rf-synchronous revolution (7.68 μs) and bunch (96 ns) trigger signals. Jitter and drift of these trigger signals are sufficiently small for use in the generation of bottom- and top triggers for the track-and-hold amp and the ADC. PIT delivers separate trigger signals for leptons and protons; the revolution trigger can be shifted in steps of 96 ns and the bunch trigger in steps of 24 ns.

The processing of these trigger signals in the monitor electronics is strongly connected to the *measurement cycle*, defined by the software of the server-PC (explained later). The trigger signal processing is a set of simple ECL-logic circuits. Signals with TTL- or NIM-levels are converted to ECL. An overview of the relevant internal trigger and analog signals is given in form of a timing diagram in Fig. 2. As shown in Fig. 1 all 4 PIT signals – revolution and bunch trigger for leptons and protons – appear first in the SYNC-stage. Here is selected, via one of the digital I/O lines[2], e^-/e^+- or p-trigger signals, dependant on the status of the accelerator. The 7.68 μs revolution trigger is used to mark the “first” bunch (n=1). The hardware is initialized by the server-PC (I/O bit: *MeasureOn*) and *synchronizes* the measurement cycle, controlled asynchronously by the PC, to the rf-synchronous PIT signals. Then SYNC opens a gate (D-FF Out) which passes the bunch trigger signals (SyncOut) to the next circuit stage. The number of bunch triggers used for the *data sampling* is software preselectable in multiples of 80 $\equiv$ 7.68 μs. The gate closes when *MeasureOn* is deactivated. The following two TRIG-stages are nearly identicaly and utilize a set of *10198* ECL one-shots. The final “bottom” and “top” trigger signals for the track-and-hold amp and the ADC board are delivered. In the future the manual “fine timing” using *10198* circuits will be made with 8-bit programmable *AD9500* delay chips, shown dashed in the hardware schematics. They allow one to shift the trigger signals, via the I/O interface board of the PC, in steps of $\approx$ 100 ps.

[2] In the prototype LPT1 was used instead of an extra I/O-board

Server-PC Hardware

The heart of the bunch current monitoring system is a commercial ADC plug-in board, which sits in the ISA (AT) bus of an IBM-compatible personal computer. This solution was prefered to microprocessor-controlled designs, as it fits better into the new PC-based control system of PETRA. The commercial ADC-board saves development time, but has to fullfil several requirements:

- A 12-bit *resolution* of the analog-to-digital converter (ADC) simplifies the analog section, because switched attenuators/amplifiers are not needed. A dynamic range of $\approx$ 74 dB of the ADC is sufficient to cover the range of bunch currents stored in the routine operation of PETRA (typically between some μA and 2 mA)

- The ADC’s *clock-rate* has to be $>$ 20 Ms/s to sample both, the bottom- and top-values within 96 ns.

- The full-scale *analog bandwidth* (or the slew-rate) of the analog signal path on the board has to be sufficient

(> 40 MHz) to settle in time (!) to the levels frozen in the track-and-hold amp.

- The *conversion time* of the ADC should not exceed 20 ns (!) over the full input range.
- The board has to offer a direct path to the *trigger (clock) input* of the ADC to allow for accelerator synchronized signal digitalization.
- The board has to offer sufficient *memory* to store the real-time digitized data for a couple of PETRA revolutions.
- The manufacturer has to offer *support* ans *documentation* for the hardware (details on signal levels, limitations of the system, etc.) as well as for the software, e.g. driver routines.

In 1994 only very few companies could present a satisfactory offer. For our first tests we ordered the *SPL 12-33* ADC plug-in board from the French company *Logisonic*. It is equipped with a *SPT7922* 12-bit ADC from *Signal Processing Technologies (SPT)*, which fullfils our requirements. After some misunderstandings we found that there was no way to feed the board with our trigger (clock!) signal. The company offered a redesign to our specifications. This was not too complicated, as changes were made only in the on-board ASIC design and not in the board layout. Our first tests in 1995 of this DESY-version of the *SPL 12-33* with the supplied driver routines were very successful. As external triggered time-domain applications with ADC's are very rare today, no specifications for the conversion time are included in the documentation. Our lab-measurements turned out $\approx$ 15 ns full-scale conversion time for the *SPL 12-33* board.

The hardware of the board is rather simple, with the analog signal buffered by a high-speed op-amp and fed into the 12-bit ADC. The trigger (clock) signal is connected through a few logic circuits to the ADC. The digitized signal is stored in a 64 kByte (32 kWord) memory. This memory, as well as all other control and data handling circuitry are housed in an ASIC.

The rest of the hardware of the server-PC is standard. For the LAN communication we use an *Elite 16* ethernet adapter board. A simple digital I/O board is added to control the trigger delay circuits by software. In the future we will use this interface for the remaining control lines, which in the prototype are accessed from the standard parallel port (LPT1) of the PC.

3 SOFTWARE OF THE SERVER-PC

All the software for the server-PC of the PETRA bunch current monitor runs under *Microsoft*'s WINDOWS 3.1. The hardware server is embedded in the PC-based control system of PETRA, whose communication is based on broadcast messages. On the PETRA LAN, all accelerator relevant information is transmitted in a *one second* rhythm into the local segment of the net. Every hardware server has to be able to update his data with this rate, but may use the received information on the status of PETRA relying on this clock rate.

The software concept of the bunch current monitor server is based on a *measurement cycle*, which should not exceed 1 s. The low-level driver routines (ADC- and I/O-board communication) are written in C++ (*Borland*), all other software (data handling, control, LAN communication, etc.) in Visual Basic (*Microsoft*). Fig. 3 shows a flowchart of the software.

Prior to the actual measurement cycle an initialization routine is executed. It is started automatically during the PC power-on cycle and initializes hardware relevant, but static settings, e.g. LPT1 port address, I/O base address of the ADC-board, etc.

After successful initialization the PC waits for an *event*. Three different events are recognized by the Visual Basic software (see the flowchart):

Exit Nothing happens and the program *exits* completely. When restarted, the initialization routine is called again.

EqmtMsg An *equipment message* event contains a dynamic control setting from an operating console (console-PC), e.g. # of PETRA revolutions to be averaged for the bunch current computations.

CycleMsg The *cycle message* is the "one second update clock" on the PETRA LAN and starts the actual measurement cycle on the bunch current monitor server-PC (see below). As described above, it contains also up-to-date information on the *status* of the accelerator. Presently we use only the *KindOfParticle* information.

Measurement Cycle

Following the flowchart of Fig. 3 the measurement cycle starts with the setting of several internal variables.
For the hardware most important is the *Sample#* information, i.e. the number of 96 ns spaced trigger pulses to be sent to the track-and-hold amp and ADC. We prefer to always store information over complete turns, in PETRA multiples of 80 bunches:

$$\text{Sample\#} = \text{Average\#} \times 160$$

For a single PETRA revolution $160 = 2 \times 80$ samples are needed to digitize the bottom- and top values of the pulse signals of the 80 possible bunches. The *Average#*, set from the operating console, gives the number of PETRA revolutions for which each bunch current value should be averaged.
Another important variable, used for the computation of the final bunch current value, is the *Sign* variable, which is based on the *KindOfParticles* variable set by the cycle message.

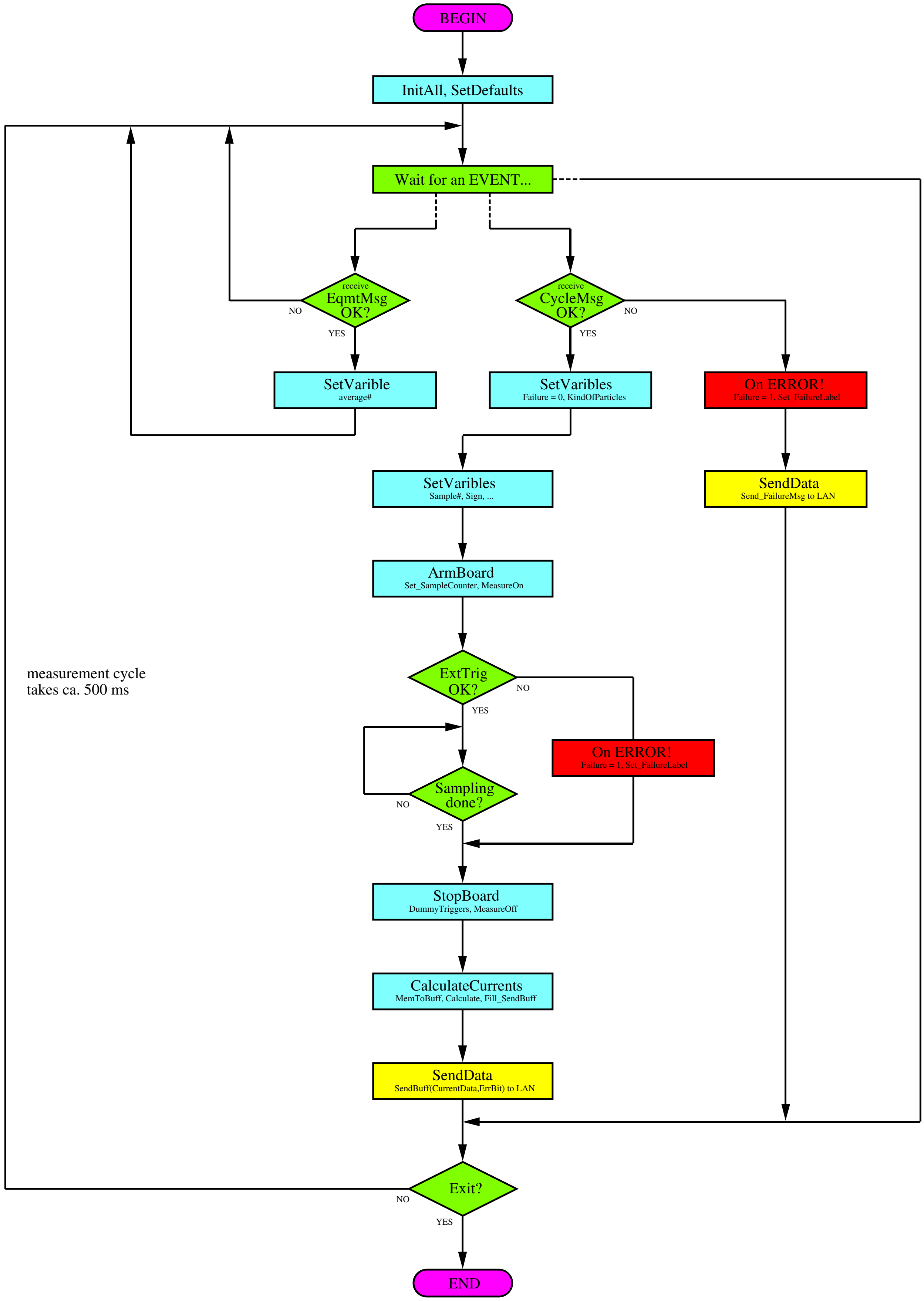

Figure 3: Flowchart of the software running on the server-PC.

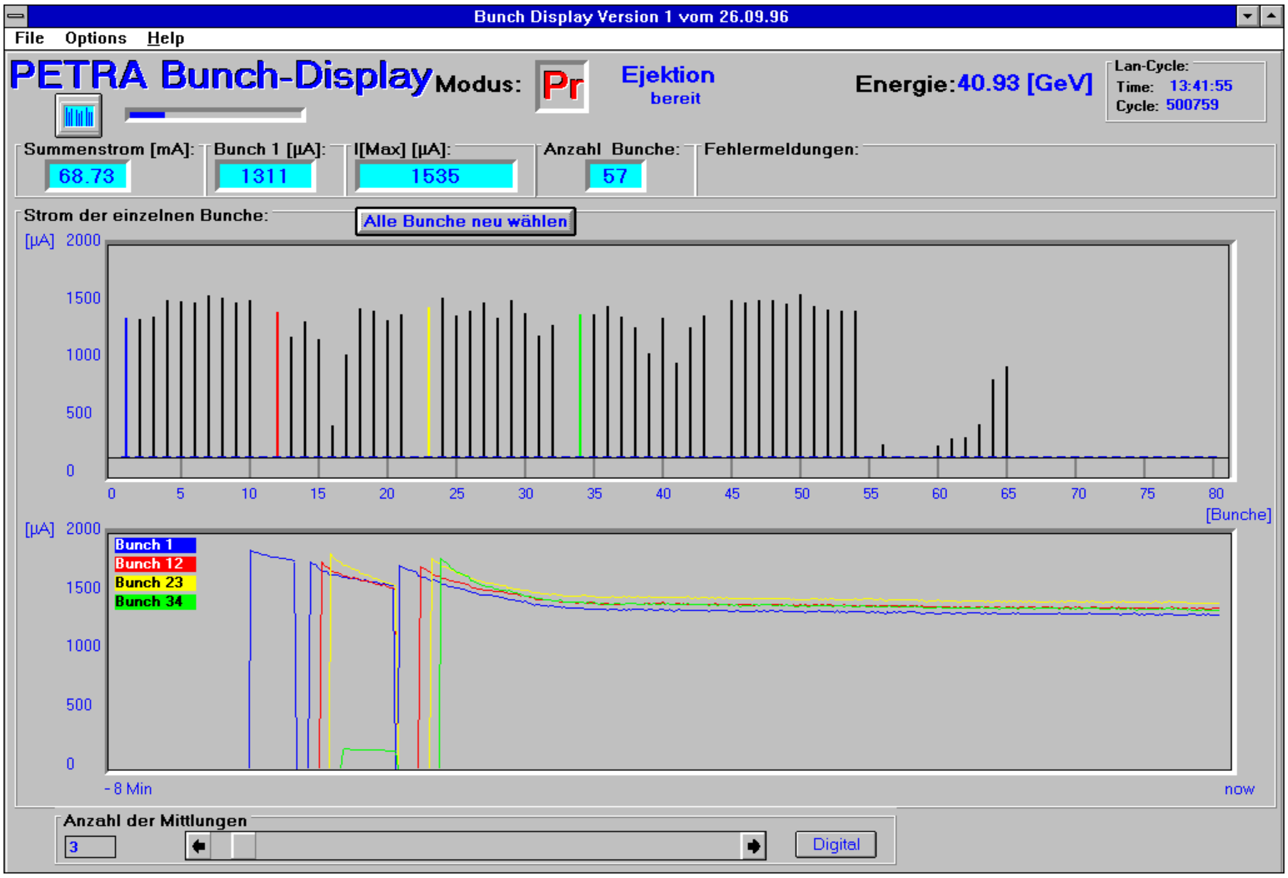

Figure 4: Operating screen on the *Petra* console of the bunch current monitor.

In the *ArmBoard* box the relevant low-level ADC-board routines are executed to enable the sampling process. The *Set_SampleCounter* command loads the *SampleCounter* register of the ACD-board with the value of *Sample#*. Finally the sampling process is started by raising the *MeasureOn* line.

With the trigger electronics enabled, the signals are generated as described in the previous chapter. In steps of 96 ns two samples are taken and stored consecutively in the *SPL 12-33* board memory. With this *realtime sampling process* the *SLP12-33 SampleCounter* is decremented with each ADC trigger pulse.
Just after starting the data sampling, the server-PC watches if the *SampleCounter* value decreases (*ExtTrig OK?*). A non-decreasing counter would be a strong hint for missing trigger signals.

The *Sampling done?* status bit of the *SPL 12-33* is automatically activated when the *SampleCounter* reaches zero. All subsequent trigger pulses are ignored by the *SPL 12-33* ADC. During the sampling process the *Sampling done?* bit is checked time-to-time asynchronously by the server-PC.

When the PC realizes that the sampling is finished (*StopBoard*), the *MeasureOn* line is deactivated. This stops the trigger signals for the ADC and track-and-hold amp within the next revolution cycle of PETRA. Finally 3 "dummy" triggers, generated (enabled) by the *SPL 12-33* low-level software (soft triggers), are sent. They are needed to take out the last digitized values from the internal data pipe conversion structure of the ADC.

Now the sampled data has to be transfered from the *SPL 12-33* to the memory of the server-PC. This is realized by mapping the board's 64 kByte memory (defined by the I/O base address) into the address space of the PC. The usual care has to be taken when choosing the base address to avoid conflicts with other hardware on the PC.

After computation of the currents of the 80 PETRA bunches (flowchart: *CalulateCurrents*) in the server-PC, the data is sent with other status information into the LAN (flowchart: *SendData*).

This measurement cycle typically takes not more than 500 ms.

4 FIRST OPERATING EXPERIENCE

The tests of the prototype started in 1995. During 1996 the device was used in the routine operation of PETRA. We still use our prototype analogue- and trigger electronics hardware. The PCB layouts are not yet finished, because we wish to integrate the known and unknown (!) "options" needed for using the instrument at the other accelerators at DESY (multi-purpose standardization).

The "softies" of DESY's control group MKI implemented an operating screen for the bunch current monitor. It is accessable via the PETRA operating console, and may also be viewed from any office-PC. Fig. 4 shows a typical proton ramp with 60 bunches in PETRA just before ejection to HERA. The display gives a bar graph of all bunches, numeric values of the total bunch current and of bunch #1 and the current vs. time plot for selected bunches.

During the commissioning of the monitor care had to be taken on the precise timing of the trigger signals. This is particularly critical for the proton operation, as they are not completely relativistic and change their speed (revolution time) during the ramp in PETRA. This effect is compensated by an extra optical fiber delay line on the analogue path.

As previously mentioned, the prototype electronics, ADC and track-and-hold amp triggers are shifted using ECL one-shots with potentiometers to their final timing value. They will be replaced with 8-bit programmable delay units, PC-controlled by the digital I/O-board.

Another little obstacle arises if the PETRA storage ring is partially filled with only a few bunches spaced by 96 ns followed by a long gap. In this case the exponential characteristic of the baseline-shift has an influence. The acquisition of the bottom value of the first bunches in this train, starting from bunch #2, is problematic as the influence of the previous pulse is still detectable. There were also problems with the measurement of empty buckets, due to noise (kicker?) on the analogue path. We decided to set very small bottom values which are aquired to zero in the server software.

5 ACKNOWLEDGEMENTS

The authors want to thank Mark Lomperski for proofreading and Willi Radloff for his contributions and helpful hints on the inductive pickup.

6 REFERENCES

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[4] S. Pätold; *private communications*